# ESE 568: Mixed Signal Design and Modeling

Lec 2: September 6th, 2017

MOS Models: Large/Small Signal



## Lecture Outline

- MOSFET (Large Signal)
  - Physical Device
  - Device Models
  - 2nd order effects
- nMOS Exercise
- Small Signal Model
  - Resistive components
  - Capacitive Components



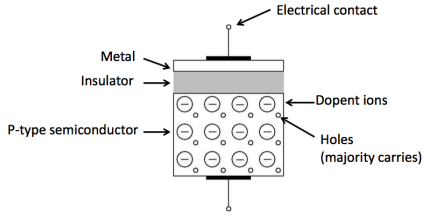
# MOSFET

Device and Models



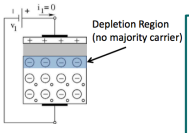
## The Operational Basis of a FET

Consider the **hypothetical** semiconductor below:
(constructed similar to a parallel plate capacitor)

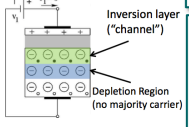





## The Operational Basis of a FET




- If we apply a voltage $v_1$ between electrodes, a charge $Q = C\,v_1$ will appear on each capacitor plate.
  - The electric field is strongest at the interface with the insulator and charge likes to accumulate there.
- Holes are pushed away from the insulator interface forming a "depletion region".
- Depth of depletion region increases with $v_1$.

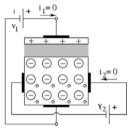



- If we increase $v_1$ above a threshold value ($V_t$), the electric field is strong enough to "pull" free electrons to the insulator interface. As the holes are repelled in this region, a "channel" is formed which contains electrons in the conduction band ("inversion layer").
- **Inversion layer is a "virtual" n-type material.**

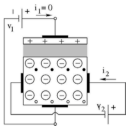


## The Operational Basis of a FET

- We apply a voltage across the p-type semiconductor: (Assume current flows only in the n-type material, ignore current flowing in the p-type semiconductor)

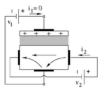


No inversion layer ($v_1 < V_t$):
- No current will flow

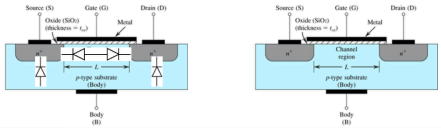


With inversion layer ($v_1 > V_t$):
- A current will flow in the channel
- Current will be proportional to electron charge in the channel or $(v_1 - V_t)$
- **Magnitude of Current $i_2$ is controlled by voltage $v_1$ (a Transistor!)**

## The Operational Basis of a FET

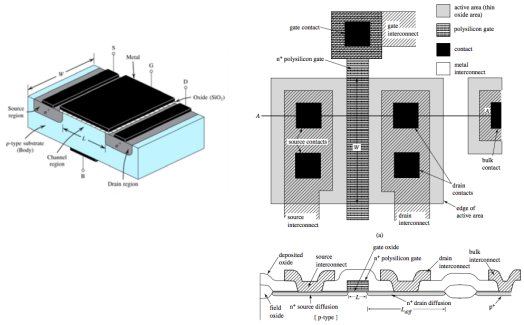


- We need to eliminate currents flowing in the p-type, i.e., current flows only in the "channel" which is a virtual n-type.






## MOSFET Physical Structure






## nMOS IV Characteristics

- To ensure that body-source and body-drain junctions are reversed bias, we assume that Body and Source are connected to each other and $v_{DS} \geq 0$.
  - *We will re-examine this assumption later*

- Without a channel, no current flows ("Cut-off").
- For $v_{GS} > V_{tn}$, a channel is formed. The total charge in the channel is

$$|Q| = CV = C_{ox} WL\,(v_{GS} - V_{tn})$$

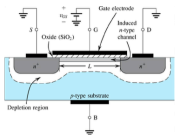
$$C = C_{ox} W L$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}: \text{ Capacitance per unit area}$$

$t_{ox}$ : Thickness of insulator

$\varepsilon_{ox}$ : permitivity of insulator

$$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.45\times10^{-11}\ \text{F/m (for } SiO_2\text{)}$$






## nMOS IV Characteristics

- $v_{GS} > V_{tn}$ : a channel is formed!
- Apply a "small" voltage, $v_{DS}$ between drain & source.
- A current flow due to the "drift" of electrons in the n-channel:

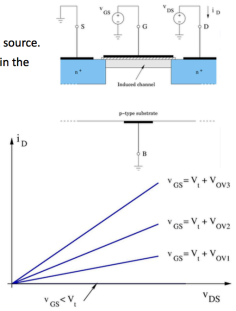
$$i_D = \mu_n C_{ox} \frac{W}{L}(v_{GS} - V_{t,n}) v_{DS}$$

$$i_D = \mu_n C_{ox} \frac{W}{L} V_{OV}\, v_{DS}$$

Overdrive Voltage: $V_{OV} = v_{GS} - V_{tn}$

MOS acts as a resistance with its conductivity controlled by $V_{OV}$ (or $v_{GS}$).

$$i_D = g_{DS} v_{DS} \quad \text{with} \quad g_{DS} = \mu_n C_{ox} \frac{W}{L} V_{OV}$$




Only valid for $v_{ds}$ near 0



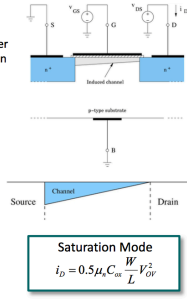
## nMOS IV Characteristics

- When $v_{DS}$ is increased the channel becomes narrower near the drain (local depth of the channel depends on the difference between $V_{OV}$ and local voltage).

Triode Mode

$$i_D = \mu_n C_{ox} \frac{W}{L}\left[V_{OV} v_{DS} - 0.5 v_{DS}^2\right]$$

- When $v_{DS}$ is increased further such that $v_{DS} = V_{OV}$, the channel depth becomes zero at the drain (Channel "pinched off").
- When $v_{DS}$ is increased further, $v_{DS} > V_{OV}$, the location of channel pinch-off remains close to the drain and $i_D$ remains approximately constant.

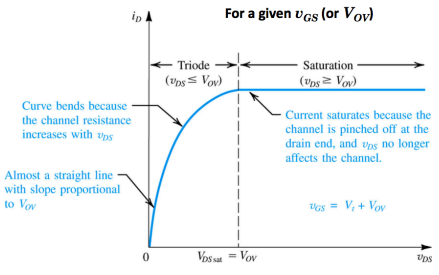



Saturation Mode

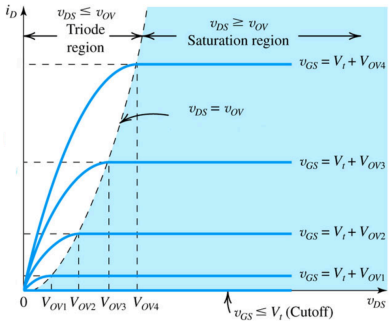
$$i_D = 0.5\mu_n C_{ox} \frac{W}{L} V_{OV}^2$$



## nMOS IV Characteristics



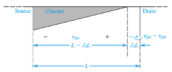
## nMOS IV Characteristics



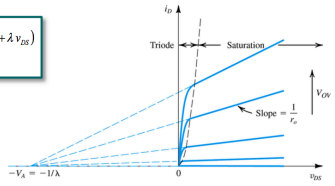



## Channel Length Modulation

- The expression we derived for saturation region assumed that the pinch-off point remains at the drain and thus $i_D$ remains constant.
- In reality, the pinch-off point moves "slightly" away from the drain: Channel-width Modulation



$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}V_{OV}^2\left(1+\lambda v_{DS}\right)$$
$$\lambda = 1/V_A$$




Define an Early Voltage

$$V_A = \frac{I_D}{\partial I_D/\partial V_{DS}}, \lambda = \frac{1}{V_A}$$



## Body Effect

- Recall that Drain-Body and Source-Body diodes should be reversed biased.
  - We assumed that Source is connected to the body ($v_{SB} = 0$) and $v_{DS} = v_{DB} > 0$
- In a chip (same body for all NMOS), it is impossible to connect all sources to the body
- Thus, the body (for NMOS) is connected to the largest negative voltage (negative terminal of the power supply).
- Doing so, changes the threshold voltage (called "Body Effect")

$$V_{tn} = V_{tn,0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$



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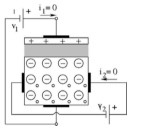
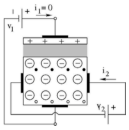


No inversion layer ($v_1 < V_t$):
- No current will flow

Not exactly



With inversion layer ($v_1 > V_t$):
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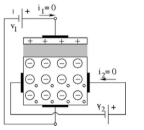
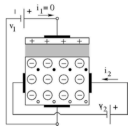


Weak Inversion ($v_1 < V_t$):
- No current will flow

Not exactly

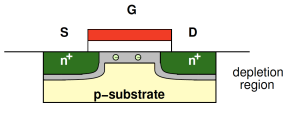


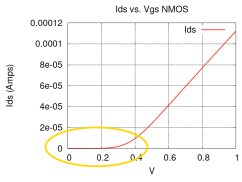
Strong Inversion ($v_1 > V_t$):
- A current will flow in the channel
- Current will be proportional to electron charge in the channel or $(v_1 - V_t)$
- **Magnitude of Current $i_2$ is controlled by voltage $v_1$ (a Transistor!)**



## Weak Inversion (or Cut-off or Subthreshold)

- Transition from insulating to conducting is non-linear, but not abrupt
- Current does flow
  - But exponentially dependent on $V_{GS}$



## Weak Inversion (or Cut-off or Subthreshold)

If $V_{GS} < V_{th}$,

$$I_{DS} = I_S \left(\frac{W}{L}\right) e^{\left(\frac{V_{GS}-V_{th}}{nkT/q}\right)} \left(1 - e^{\left(\frac{V_{DS}}{-kT/q}\right)}\right)\left(1 + \lambda V_{DS}\right)$$

- Current is from the parasitic NPN BJT transistor when gate is unbiased and there is no conducting channel

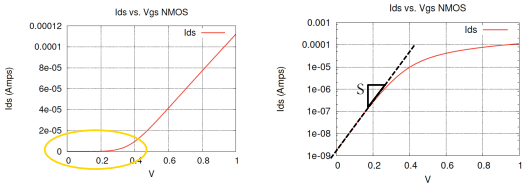


## Subthreshold Slope

- Exponent in $V_{GS}$ determines how steep the turnon is

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

  - Units: V/dec
  - Every S Volts, $I_{DS}$ is scaled by factor of 10






## 2nd Order Effects

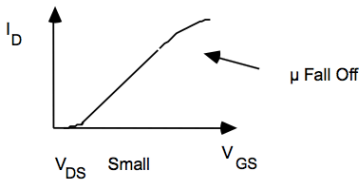
- Mobility Degradation with Normal Field
  - Vertical field
  - Triode and saturation region
- Velocity Saturation
  - Lateral field
  - Saturation region
- Short Channel Effects



## Mobility Degradation with Normal Field

**Usually Modeled Empirically**

**Affects both saturation and triode regions, strong inversion only**






## Mobility Degradation with Normal Field

- High gate-to-source voltage

$$\mu_n(eff) \approx \frac{\mu_{n0}}{1 + \theta(V_{GS} - V_T)}$$

- $\theta$ = mobility modulation factor (empirical)



## Velocity Saturation

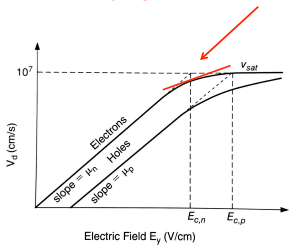
**Affects saturation region in strong inversion**

Normally, $v = \mu E$ but if $E > E_{CRIT}$ Then $v = v_{SAT}$

## Velocity Saturation

- Once velocity saturates:

Mobility degradaion due to lateral electric field ($V_{DS}/L_{eff}$)






## Velocity Saturation

**Affects saturation region in strong inversion**

Normally, $v = \mu E$ but if $E > E_{CRIT}$ Then $v = v_{SAT}$

Qualitatively

$I_D = WQ_N v$

Below Critical Field (Long Channel) For $V_{DS} > V_{DSAT}$

$Q_N \propto V_{GS} - V_T$

$v \propto E \propto V_{GS} - V_T$

Thus $I_D \propto (V_{GS} - V_T)^2$



## Velocity Saturation

**Affects saturation region in strong inversion**

Normally, $v = \mu E$ but if $E > E_{CRIT}$ Then $v = v_{SAT}$

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$I_D = WQ_N v$

Below Critical Field (Long Channel) For $V_{DS} > V_{DSAT}$

$Q_N \propto V_{GS} - V_T$

$v \propto E \propto V_{GS} - V_T$

Thus $I_D \propto (V_{GS} - V_T)^2$

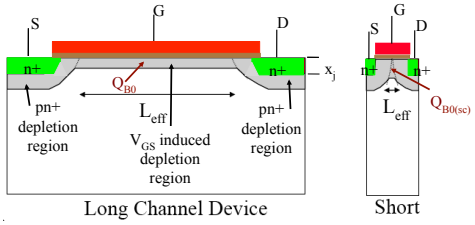
High Field (Short Channel)

If $v \rightarrow v_{SAT}$ then $v$ is constant

$I_D \propto (V_{GS} - V_T)$



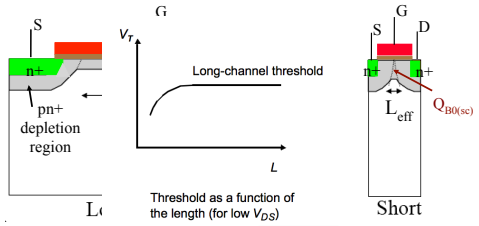
## Short Channel Effects – $V_T$ Reduction




$V_{T0}$ (short channel) = $V_{T0}$ - $\Delta V_{T0}$



## Short Channel Effects – $V_T$ Reduction

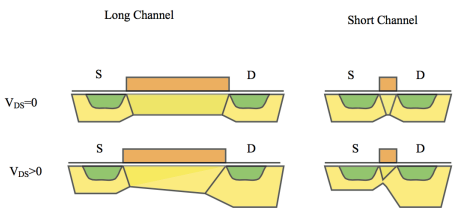



$V_{T0}$ (short channel) = $V_{T0}$ - $\Delta V_{T0}$



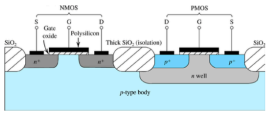
## Short Channel Effects - DIBL

- Drain Induced Barrier Lowering
  - $V_T$ Reduction with Drain Bias



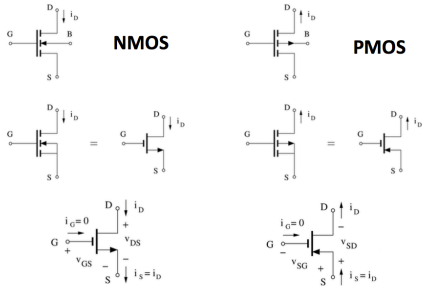
## pMOS Device

- A PMOS can be constructed analogous to an NMOS: (n-type body), heavily doped p-type source and drain.
- A virtual "p-type" channel is formed in a P-MOS (holes are carriers in the channel) by applying a negative $v_{GS}$.
- i-v characteristic equations of a PMOS is similar to the NMOS with the exception:
  - Voltages are negative (we switch the terminals to have positive voltages: use $v_{SG}$ instead of $v_{GS}$).
  - Use mobility of holes, $\mu_p$, instead of $\mu_n$ in the expression for $i_D$






## MOS Circuit Symbols






## MOS IV Characteristic Equations

Not exactly, subT current flows

**NMOS** $(V_{OV} = v_{GS} - V_{tn}, \lambda = 1/V_A)$

| | | |
|---|---|---|
| Cut-Off : | $V_{OV} \le 0$ | $i_D = 0$ |
| Triode : | $V_{OV} \ge 0$ and $v_{DS} \le V_{OV}$ | $i_D = 0.5\mu_n C_{ox} \frac{W}{L}\left[2V_{OV}v_{DS} - v_{DS}^2\right]$ |
| Saturation : | $V_{OV} \ge 0$ and $v_{DS} \ge V_{OV}$ | $i_D = 0.5\mu_n C_{ox} \frac{W}{L} V_{OV}^2[1+\lambda(v_{DS}-V_{OV})]$ |

**PMOS** $(V_{OV} = v_{SG} - |V_{tp}|, \lambda = 1/|V_A|)$*

| | | |
|---|---|---|
| Cut-Off : | $V_{OV} \le 0$ | $i_D = 0$ |
| Triode : | $V_{OV} \ge 0$ and $v_{SD} \le V_{OV}$ | $i_D = 0.5\mu_p C_{ox} \frac{W}{L}\left[2V_{OV}v_{SD} - v_{SD}^2\right]$ |
| Saturation : | $V_{OV} \ge 0$ and $v_{SD} \ge V_{OV}$ | $i_D = 0.5\mu_p C_{ox} \frac{W}{L} V_{OV}^2[1+\lambda(v_{DS}-V_{OV})]$ |

Simplified for hand analysis



## nMOS Exercise

- http://www-g.eng.cam.ac.uk/mmg/teaching/linearcircuits/mosfet.html



## Small Signal Models


## Formal Derivation of Small Signal Model

- Signal + Bias for element A $(i_A, v_A)$ : $i_A = f(v_A)$
- Bias for element A $(I_A, V_A)$ : $I_A = f(V_A)$
- Signal for element A $(i_a, v_a)$ : $i_a = g(v_a)$

## Formal Derivation of Small Signal Model

- Signal + Bias for element A ($i_A$, $v_A$) : $i_A = f(v_A)$
- Bias for element A ($I_A$, $V_A$) : $I_A = f(V_A)$
- Signal for element A ($i_a$, $v_a$) : $i_a = g(v_a)$

$$i_A = f(v_A)$$
$$= f(V_A) + f^{(1)}(V_A)\cdot(v_A - V_A) + \frac{f^{(2)}(V_A)}{2!}\cdot(v_A - V_A)^2 + \ldots \quad \text{(Taylor Series Expansion)}$$
$$= f(V_A) + f^{(1)}(V_A)\cdot v_a + \frac{f^{(2)}(V_A)}{2!}\cdot v_a{}^2 + \ldots$$
$$\approx f(V_A) + f^{(1)}(V_A)\cdot v_a$$
$$i_A = i_a + I_A = I_A + f^{(1)}(V_A)\cdot v_a$$

$$i_a = g(v_a) = f^{(1)}(V_A)\cdot v_a$$

**Small signal means:**

$$\left|f^{(1)}(V_A)\cdot v_a\right| >> \left|\frac{f^{(2)}(V_A)}{2!}\cdot v_a{}^2\right|$$
$$\left|v_a\right| << 2\cdot\left|\frac{f^{(1)}(V_A)}{f^{(2)}(V_A)}\right|$$



## MOS Small Signal Model

MOS iv equations: $i_D = f(v_{GS}, v_{DS})$, $i_G = 0$

- Signal + Bias for MOS ($i_D$, $v_{GS}$ , $v_{DS}$) : $i_D = f(v_{GS}, v_{DS})$, $i_G = 0$
- Bias for MOS ($I_D$, $V_{GS}$ , $V_{DS}$) : $I_D = f(V_{GS}, V_{DS})$, $I_G = 0$
- Signal for MOS ($i_d$, $v_{gs}$ , $v_{ds}$) : $i_d = g(v_{gs}, v_{ds})$, $i_g = 0$



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MOS iv equations: $i_D = f(v_{GS}, v_{DS})$, $i_G = 0$

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- Bias for MOS ($I_D$, $V_{GS}$ , $V_{DS}$) : $I_D = f(V_{GS}, V_{DS})$, $I_G = 0$
- Signal for MOS ($i_d$, $v_{gs}$ , $v_{ds}$) : $i_d = g(v_{gs}, v_{ds})$, $i_g = 0$

$$I_D + i_d = i_D = f(v_{GS}, v_{DS}) \quad \text{(Taylor Series Expansion in 2 variables)}$$
$$= f(V_{GS}, V_{DS}) + \left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}}\cdot(v_{GS} - V_{GS}) + \left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}}\cdot(v_{DS} - V_{DS}) + \ldots$$
$$\approx I_D + \left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}}\times v_{gs} + \left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}}\times v_{ds}$$

$$i_d \approx \left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}}\times v_{gs} + \left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}}\times v_{ds}$$



## MOS Small Signal Model

$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS}) = f(v_{GS}, v_{DS})$$
$$i_d = \left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}}\cdot v_{gs} + \left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}}\cdot v_{ds}$$



## MOS Small Signal Model

$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS}) = f(v_{GS}, v_{DS})$$
$$i_d = \left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}}\cdot v_{gs} + \left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}}\cdot v_{ds}$$
$$\left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} = 2\times 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)(1 + \lambda v_{DS})\Big|_{V_{GS},V_{DS}}$$



## MOS Small Signal Model

$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS}) = f(v_{GS}, v_{DS})$$
$$i_d = \left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}}\cdot v_{gs} + \left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}}\cdot v_{ds}$$
$$\left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} = 2\times 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)(1 + \lambda v_{DS})\Big|_{V_{GS},V_{DS}}$$
$$= 2\times\frac{0.5\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})}{(V_{GS} - V_t)} = \frac{2I_D}{V_{OV}} \equiv g_m$$

## MOS Small Signal Model

$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS}) = f(v_{GS}, v_{DS})$$

$$\left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}} = \lambda \times 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)^2\Big|_{V_{GS},V_{DS}}$$

$$= \lambda \times \frac{0.5\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2}{}$$



## MOS Small Signal Model

$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS}) = f(v_{GS}, v_{DS})$$

$$\left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}} = \lambda \times 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)^2\Big|_{V_{GS},V_{DS}}$$

$$= \lambda \times \frac{0.5\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})}{(1+\lambda V_{DS})} = \frac{\lambda I_D}{(1+\lambda V_{DS})} \approx \lambda I_D \equiv \frac{1}{r_o}$$



## MOS Small Signal Model

$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS}) = f(v_{GS}, v_{DS})$$

$$i_d = \left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} \cdot v_{gs} + \left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}} \cdot v_{ds}$$

$$\left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} = 2\times 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)(1+\lambda v_{DS})\Big|_{V_{GS},V_{DS}}$$

$$= 2\times\frac{0.5\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})}{(V_{GS}-V_t)} = \frac{2I_D}{V_{OV}} \equiv g_m$$

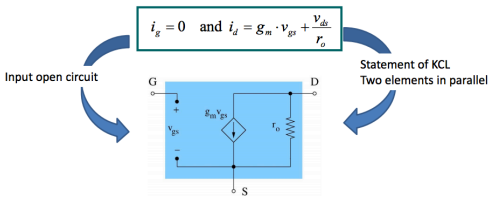
$$\left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}} = \lambda \times 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)^2\Big|_{V_{GS},V_{DS}}$$

$$= \lambda \times \frac{0.5\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})}{(1+\lambda V_{DS})} = \frac{\lambda I_D}{(1+\lambda V_{DS})} \approx \lambda I_D \equiv \frac{1}{r_o}$$

$$\boxed{i_d = g_m \cdot v_{gs} + \frac{v_{ds}}{r_o} \qquad i_g = 0}$$



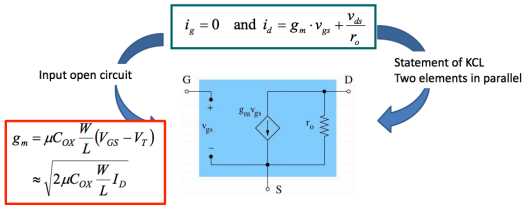
## MOS Small Signal Model




$$\boxed{g_m = \frac{2\cdot I_D}{V_{OV}}} \qquad \boxed{r_o \approx \frac{1}{\lambda \cdot I_D}} \qquad \boxed{g_m r_o = \frac{2}{\lambda V_{OV}} = \frac{2V_A}{V_{OV}} >> 1}$$



## MOS Small Signal Model




$$\boxed{g_m = \mu C_{OX}\frac{W}{L}(V_{GS}-V_T) \approx \sqrt{2\mu C_{OX}\frac{W}{L}I_D}} \qquad \boxed{g_m = \frac{2\cdot I_D}{V_{OV}}} \qquad \boxed{r_o \approx \frac{1}{\lambda \cdot I_D}} \qquad \boxed{g_m r_o = \frac{2}{\lambda V_{OV}} = \frac{2V_A}{V_{OV}} >> 1}$$



## Back Gate Small Signal Model

$$g_{mb} \equiv \frac{\partial I_{DS}}{\partial V_{BS}} = \frac{\partial I_{DS}}{\partial V_T}\frac{\partial V_T}{\partial V_{BS}} \text{ at o.p.}$$

$$g_{mb} = \frac{\partial}{\partial V_T}\frac{\mu C_{OX}}{2}\frac{W}{L}(V_{GS}-V_T)^2\frac{\partial V_T}{\partial V_{BS}} = \mu C_{OX}\frac{W}{L}(V_{GS}-V_T)\frac{\partial V_T}{\partial V_{SB}}$$

$$= g_m\frac{\partial V_T}{\partial V_{SB}}$$

Since $V_T = V_{T0} + \gamma\left(\sqrt{2|\phi_{Fip}|+V_{SB}} - \sqrt{2|\phi_{Fip}|}\right)$

$$\frac{\partial V_T}{\partial V_{SB}} = \frac{\gamma}{2}\frac{1}{\sqrt{2|\phi_{Fip}|+V_{SB}}}$$

$$\boxed{\therefore g_{mb} = g_m\frac{\gamma}{2\sqrt{2|\phi_{Fip}|+V_{SB}}}} \text{ where } \gamma = \frac{\sqrt{2q\varepsilon N_A}}{C_{OX}}$$

## Back Gate Small Signal Model

$$g_{mb} \equiv \frac{\partial I_{DS}}{\partial V_{BS}} = \frac{\partial I_{DS}}{\partial V_T}\frac{\partial V_T}{\partial V_{BS}} \text{ at o.p.}$$

$$g_{mb} = \frac{\partial}{\partial V_T}\frac{\mu C_{OX}}{2}\frac{W}{L}(V_{GS}-V_T)^2\frac{\partial V_T}{\partial V_{BS}} = \mu C_{OX}\frac{W}{L}(V_{GS}-V_T)\frac{\partial V_T}{\partial V_{SB}}$$

$$= g_m\frac{\partial V_T}{\partial V_{SB}}$$

Since $V_T = V_{T0} + \gamma\left(\sqrt{2|\phi_{Fip}| + V_{SB}} - \sqrt{2|\phi_{Fip}|}\right)$

$$\frac{\partial V_T}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2|\phi_{Fip}| + V_{SB}}}$$

$$\therefore g_{mb} = g_m\frac{\gamma}{2\sqrt{2|\phi_{Fip}| + V_{SB}}} \text{ where } \gamma = \frac{\sqrt{2q\varepsilon N_A}}{C_{OX}}$$

$$i_d = g_m \cdot v_{gs} + \frac{v_{ds}}{r_o} + g_{mb} \cdot v_{sb}$$

$$g_s = g_{mb}$$



## Weak Inversion Small Signal Model

$I_D \propto e^{q\Psi_S/kT}$

Recall $\Delta\Psi_S = \frac{C_{OX}}{C_{OX}+C_B}\Delta V_{GS} = \frac{\Delta V_{GS}}{n}$; capacitive voltage divider

$n = \frac{C_{OX}+C_S}{C_{OX}}$ $C_S = \frac{dQ_S}{d\Psi_S} = \sqrt{\frac{q\varepsilon N_A}{2\Psi_S}}$ Typical n ~1.5-1.6

$I \propto e^{qV_{GS}/nkT}$

which leads to $I_D = I_0 e^{qV_{GS}/nkT}(1+\lambda V_{DS})$

$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = \frac{qI_D}{nkT}$; similar to BJT

$r_o = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} \approx \frac{1}{\lambda I_D}$; same as in strong inv.



## Weak Inversion Small Signal Model

$$I_D \propto e^{q(V_{GS}-V_T)/nkT}$$

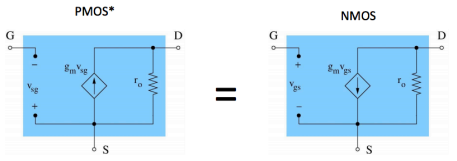
$$g_{mb} \equiv \frac{\partial I_{DS}}{\partial V_{BS}} = \frac{\partial I_{DS}}{\partial V_T}\frac{\partial V_T}{\partial V_{BS}} = -g_m\frac{\partial V_T}{\partial V_{BS}}$$

$$\frac{\partial V_T}{\partial V_{BS}} = -\frac{\gamma}{2\sqrt{2|\phi_{Fip}| + V_{SB}}}$$ as in strong inversion

$$g_{mb} \approx g_m\frac{\gamma}{2\sqrt{2|\phi_{Fip}| + V_{SB}}}$$ same as in strong inversion



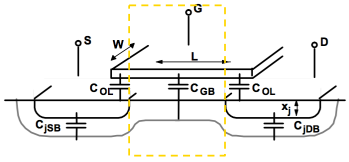
## pMOS Small Signal Model




- **PMOS small-signal circuit model is identical to NMOS**
  - We will use NMOS circuit model for both!
  - For both NMOS and PMOS, while $i_D \geq 0$ and $I_D \geq 0$, signal quantities: $i_d$, $v_{gs}$, and $v_{ds}$, can be negative!



## MOSFET Parasitic Capacitance

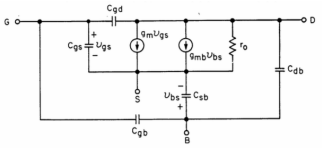



- Any two conductors separated by an insulator form a parallel-plate capacitor
- Two types
  - Extrinsic – Outside the box (e.g. junction, overlap)
  - Intrinsic – Inside the box (e.g. gate-to-channel)



## Capacitance Roundup

- $C_{gs} = C_{GSi} + C_{GSO}$
- $C_{gd} = C_{GDi} + C_{GDO}$
- $C_{gb} = C_{GBO}$
- $C_{sb} = C_{diff}$
- $C_{db} = C_{diff}$




intrinsic
extrinsic

## Extrinsic Capacitance Roundup

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- $C_{gd}=C_{GDO}$
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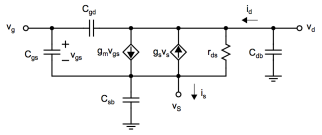


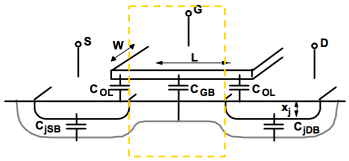

extrinsic



## Extrinsic Capacaitors




## MOSFET Parasitic Capacitance

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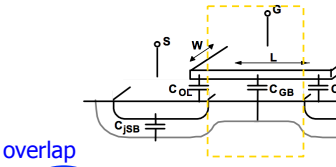
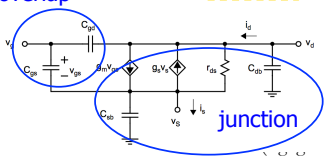
## MOSFET Parasitic Capacitance




overlap




junction

y an insulator form

nction, overlap)

-to-channel)



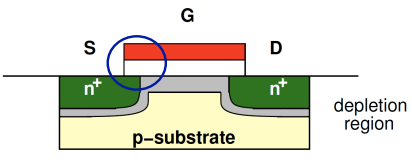
## Extrinsic

Overlap Capacitance




## Overlap

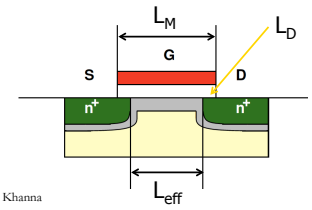
- gate/source and gate/drain overlap



## Overlap

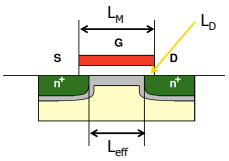
- Length of overlap

$$L_D = \frac{L_M - L_{eff}}{2}$$






## Overlap Capacitance

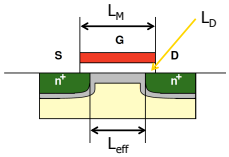



$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$

$$C_o = \varepsilon_{ox} \frac{WL_D}{t_{ox}}$$



## Overlap Capacitance




$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$

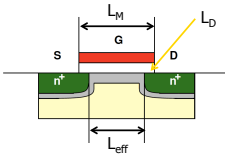
$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

$$C_o = \varepsilon_{ox} \frac{WL_D}{t_{ox}}$$

$$C_o = C_{ox} WL_D$$



## Overlap Capacitance




$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

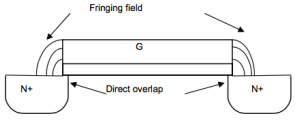
$$C_o = \varepsilon_{ox} \frac{WL_D}{t_{ox}}$$

$$C_o = C_{ox} WL_D = C_{GSO} = C_{GDO}$$



## Use Measured Values

Gate to drain and gate to source overlap capacitance




$C_{GDO}$ (or $C_{GSO}$) $= WC_{gso}$

For best results, use measured value of $C_{gso}$.



## Overlap Capacitance

| Name | Model Parameters | Units |
|---|---|---|
| LEVEL | Model type (1, 2, or 3) | |
| CBD | Bulk-drain zero-bias p-n cap (not used) | F |
| CBS | Bulk-source zero-bias p-n cap (not used) | F |
| CJ | Bulk p-n zero-bias bottom cap/area | F/m**2 |
| CJSW | Bulk p-n zero-bias perimeter cap/length | F/m |
| MJ | Bulk p-n bottom grading coefficient | |
| MJSW | Bulk p-n sidewall grading coefficient | |
| FC | Empirical bulk p-n forward-bias cap coefficient | |
| CGSO | Gate-source overlap cap/channel width | F/m |
| CGDO | Gate-drain overlap cap/channel width | F/m |
| CGBO | Gate-bulk overlap cap/channel width | F/m |
| NSUB | Substate doping density | 1/cm**3 |
| NSS | Surface-state density | 1/cm**2 |
| NFS | Fast surface-state density | 1/cm**2 |
| TOX | Oxide thickness | m |
| TPG | Gate material type:<br>+ 1 = opposite of substrate,<br>- 1 = same as substrate,<br>0 = aluminum | |
| XJ | Metallurgical junction depth | m |

Scales with Width (W)

## Extrinsic

Junction Capacitance

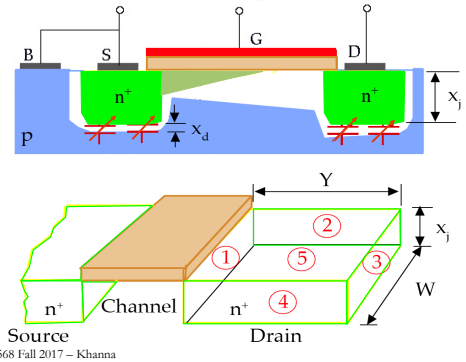


## Diode Capacitance

- When a reverse voltage is applied to a PN junction, a depletion region containing almost no charge carriers is generated and acts similarly to the dielectric of a capacitor.
- The depletion region increases in width as the reverse voltage across it increases.
- If we imagine that the diode capacitance can be likened to a parallel plate capacitor, then as the plate spacing (i.e. the depletion region width) increases, the capacitance should decrease.
- Increasing the reverse bias voltage across the PN junction therefore decreases the diode capacitance.
- Worst case is in zero-bias case



## Junction Capacitance






## Juntion Capacitance

$$C_{js} = \frac{C_{j0}}{\sqrt{1 + \frac{V_{SB}}{\Phi_0}}} \qquad C_{j\text{-}sw} = \frac{C_{j\text{-}sw0}}{\sqrt{1 + \frac{V_{SB}}{\Phi_0}}} \qquad \psi_0 = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}$$

$$C_{sb} = A_s C_{js} + P_s C_{j\text{-}sw}$$

1. Source-substrate bottom wall $A_S \times C_j$
2. Source-substrate side wall $P_S \times C_{jsw}$
3. Channel-substrate: too complicated for hand calculation- ignore



## Juntion Capacitance

$$C_{jd} = \frac{C_{j0}}{\sqrt{1 + \frac{V_{DB}}{\Phi_0}}} \qquad C_{j\text{-}sw} = \frac{C_{j\text{-}sw0}}{\sqrt{1 + \frac{V_{SB}}{\Phi_0}}} \qquad \psi_0 = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}$$

$$C_{db} = A_d C_{jd} + P_d C_{j\text{-}sw}$$

1. Drain-substrate bottom wall $A_D \times C_j$
2. Drain-substrate side wall $P_D \times C_{jsw}$



## Junction Capacitance

| Name | Model Parameters | Units |
|---|---|---|
| LEVEL | Model type (1, 2, or 3) | |
| CBD | Bulk-drain zero-bias p-n cap (not used) | F |
| CBS | Bulk-source zero-bias p-n cap (not used) | F |
| CJ | Bulk p-n zero-bias bottom cap/area | F/m**2 |
| CJSW | Bulk p-n zero-bias perimeter cap/length | F/m |
| MJ | Bulk p-n bottom grading coefficient | |
| MJSW | Bulk p-n sidewall grading coefficient | |
| FC | Empirical bulk p-n forward-bias cap coefficient | |
| CGSO | Gate-source overlap cap/channel width | F/m |
| CGDO | Gate-drain overlap cap/channel width | F/m |
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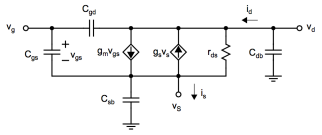
| NSUB | Substate doping density | 1/cm**3 |
| NSS | Surface-state density | 1/cm**2 |
| NFS | Fast surface-state density | 1/cm**2 |
| TOX | Oxide thickness | m |
| TPG | Gate material type:<br>+ 1 = opposite of substrate,<br>- 1 = same as substrate,<br>0 = aluminum | |
| XJ | Metallurgical junction depth | m |

Scales with Junction area or width

## Extrinsic Capacitance Roundup

- $C_{gs}=C_{GSO}$
- $C_{gd}=C_{GDO}$
- $C_{sb}=C_{diff}$
- $C_{db}=C_{diff}$

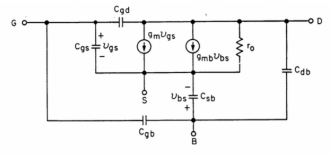



extrinsic



## Intrinsic Capacitance Roundup

- $C_{gs}=C_{GSi}$
- $C_{gd}=C_{GDi}$
- $C_{gb}=C_{GBO}$




intrinsic



## Intrinsic Capacitances

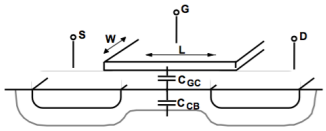


## Gate-to-Bulk Capacitance

- When talking about gate capacitance, we must distinguish several operating regions
  - Transistor on
    - Triode and saturation regions
  - Transistor "off"
    - Subthreshold operation



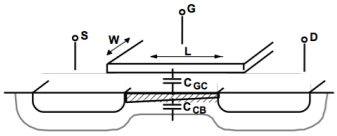
## Gate-to-Bulk Capacitance – Subthreshold




- There is no conductive channel
  - Gate sees a capacitor to substrate, equivalent to the series combination of the gate oxide capacitor and the depletion capacitance
  - $C_{GC} = WLC_{ox}$

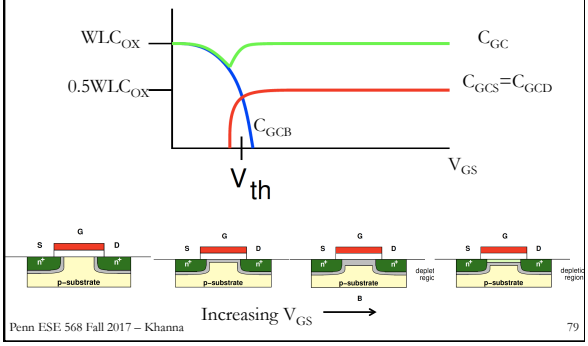


## Gate-to-Bulk Capacitance – Triode



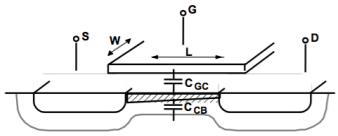

- Gate terminal and conductive channel form a parallel plate capacitor across gate oxide $C_{GC} = WLC_{ox}$ (lumped into $C_{GS}$ and $C_{GD}$)
- The depletion capacitance $C_{CB}$ adds extra capacitance from drain and source to substrate
  - Usually negligible

## Capacitance vs $V_{GS}$ ($V_{DS}$=0)






## Gate-to-Bulk Capacitance – Saturation




- The "bottom plate" of the capacitor does not change uniformly
- Analysis shows that in this case $C_{GS}$=2/3WLCox



## Intrinsic $C_{gs}$

$$C_{GSi} = \frac{\partial Q_T}{\partial V_{GS}}$$

$$Q_T = WC_{OX}\int_0^L (V_{GS} - V_T - V(y))dy$$ : total integrated inversion charge

We do not know V(y) as a function of y. Instead, from Lecture 1;

$$W\mu C_{OX}(V_{GS} - V_T - V(y))dV(y) = I_D dy$$

Rearranging,

$$dy = dV(y)\frac{W\mu C_{OX}(V_{GS} - V_T - V(y))}{I_D}$$

$$Q_T = \frac{W^2 C_{OX}^2 \mu}{I_D}\int_0^{V_{GS}-V_T}(V_{GS} - V_T - V(y))^2 dV(y)$$

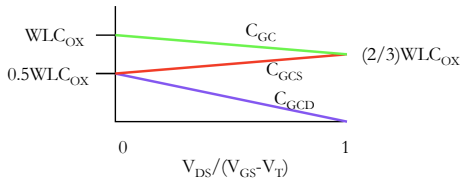
$$= WLC_{OX}\frac{2}{3}(V_{GS} - V_T)$$

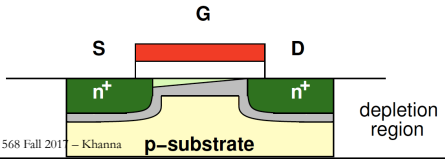
$$\boxed{C_{GSi} = \frac{2}{3}WLC_{OX}}$$

$C_{gs}=C_{GSi}+C_{GSO}$



## Saturation Capacitance






## First Order Capacitance Summary

| Opearation Region | $C_{GCB}$ | $C_{GCS}$ | $C_{GCD}$ | $C_{GC}$ | $C_G$ |
|---|---|---|---|---|---|
| Subthreshold | | | | | |
| Linear | | | | | |
| Saturation | | | | | |



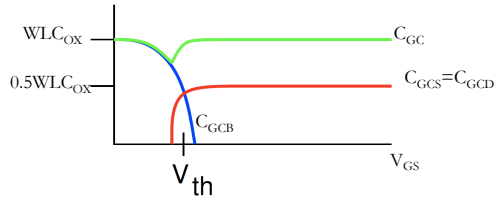
## First Order Capacitance Summary

| Opearation Region | $C_{GCB}$ | $C_{GCS}$ | $C_{GCD}$ | $C_{GC}$ | $C_G$ |
|---|---|---|---|---|---|
| Subthreshold | | | | | |
| Linear | 0 | $C_{OX}WL/2$ | $C_{OX}WL/2$ | | |
| Saturation | | | | | |

$$C_{GCS} = C_{GCD} = \frac{1}{2}C_{ox}WL_{effective}$$

## First Order Capacitance Summary

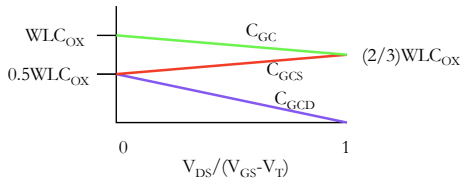
| Operation Region | $C_{GCB}$ | $C_{GCS}$ | $C_{GCD}$ | $C_{GC}$ | $C_G$ |
|---|---|---|---|---|---|
| Subthreshold | $C_{OX}WL$ | 0 | 0 | | |
| Linear | 0 | $C_{OX}WL/2$ | $C_{OX}WL/2$ | | |
| Saturation | | | | | |






## First Order Capacitance Summary

| Operation Region | $C_{GCB}$ | $C_{GCS}$ | $C_{GCD}$ | $C_{GC}$ | $C_G$ |
|---|---|---|---|---|---|
| Subthreshold | $C_{OX}WL$ | 0 | 0 | | |
| Linear | 0 | $C_{OX}WL/2$ | $C_{OX}WL/2$ | | |
| Saturation | 0 | $(2/3)C_{OX}WL$ | 0 | | |






## First Order Capacitance Summary

| Operation Region | $C_{GCB}$ | + | $C_{GCS}$ | + | $C_{GCD}$ | = | $C_{GC}$ | $C_G$ |
|---|---|---|---|---|---|---|---|---|
| Subthreshold | $C_{OX}WL$ | | 0 | | 0 | | $C_{OX}WL$ | |
| Linear | 0 | | $C_{OX}WL/2$ | | $C_{OX}WL/2$ | | $C_{OX}WL$ | |
| Saturation | 0 | | $(2/3)C_{OX}WL$ | | 0 | | $(2/3)C_{OX}WL$ | |



## First Order Capacitance Summary

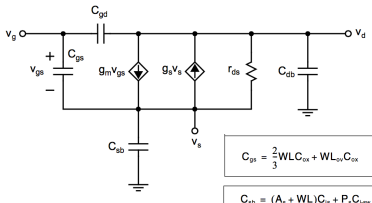
| Operation Region | $C_{GCB}$ | $C_{GCS}$ | $C_{GCD}$ | $C_{GC}$ | $C_G$ |
|---|---|---|---|---|---|
| Subthreshold | $C_{OX}WL$ | 0 | 0 | $C_{OX}WL$ | $C_{OX}WL+2C_O$ |
| Linear | 0 | $C_{OX}WL/2$ | $C_{OX}WL/2$ | $C_{OX}WL$ | $C_{OX}WL+2C_O$ |
| Saturation | 0 | $(2/3)C_{OX}WL$ | 0 | $(2/3)C_{OX}WL$ | $(2/3)C_{OX}WL+2C_O$ |

$$C_o = \frac{1}{2}C_{ox}W\left(L_{drawn} - L_{effective}\right) = C_{GSO} = C_{GDO}$$



## Small Signal Capacitance Roundup

- Textbook pgs 41 and 42



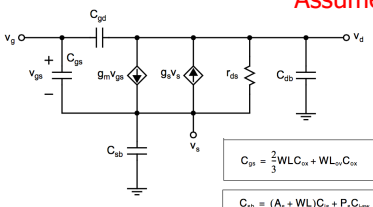

| | |
|---|---|
| $C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox}$ | $C_{gd} = WL_{ov}C_{ox}$ |
| $C_{sb} = (A_s + WL)C_{js} + P_sC_{jsw}$ | $C_{js} = \frac{C_{j0}}{\sqrt{1 + V_{SB}/\Phi_0}}$ |
| $C_{db} = A_dC_{jd} + P_dC_{jsw}$ | $C_{jd} = \frac{C_{j0}}{\sqrt{1 + V_{DB}/\Phi_0}}$ |



## Small Signal Capacitance Roundup

- Textbook pgs 41 and 42

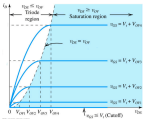
Assumes Saturation

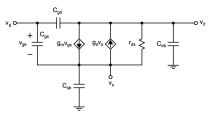



| | |
|---|---|
| $C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox}$ | $C_{gd} = WL_{ov}C_{ox}$ |
| $C_{sb} = (A_s + WL)C_{js} + P_sC_{jsw}$ | $C_{js} = \frac{C_{j0}}{\sqrt{1 + V_{SB}/\Phi_0}}$ |
| $C_{db} = A_dC_{jd} + P_dC_{jsw}$ | $C_{jd} = \frac{C_{j0}}{\sqrt{1 + V_{DB}/\Phi_0}}$ |

## Lecture Outline

- MOSFET has modes of operation
  - Subthreshold
  - Triode
  - Saturation
- Small Signal Model
  - Enables hand analysis
  - Resistive components
    - $g_m$, $r_o$
  - Capacitive Components
    - Dependent on modes of operation, but well defined model for saturation, which is where we want to design our transistors to be







## Admin

- HW 1 due Friday at midnight in Canvas
  - You should be able to do it all now
  - Sets up the Cadence environment and gets you familiar with Cadence basics