ALC4050
(PN: ALC4050-VA1-CG)

AUDIO CODEC WITH USB TO I2S AUDIO CONTROLLER AND HARDWARE ACTIVE NOISE CANCELLATION

DATASHEET

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC4050 Audio Codec.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2018/11/19	First release.
1.1	2019/05/02	Modify hardware EQ function for playback path
1.2	2019/05/13	Typo corrections

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1. General Description

The ALC4050 is a single-chip USB 2.0 audio codec with embedded USB 2.0 to I2S and SPDIF interface for high analog and digital audio performance. The ALC4050 integrates stereo analog input and output, USB, I2S, I2C, digital microphone, and SPDIF interfaces to support a standard USB audio device class designed for all major commercial operating systems, e.g., Windows, Linux, and Android.

The ALC4050 features a Class-G type ultra-low-power cap-saving headphone amplifier. It is a high efficiency audio amplifier with an integrated Class-G voltage converter that enhances efficiency at low output power. The ALC4050 integrates a USB 2.0 function controller and USB transceiver optimized for a high data transfer rate, a high speed MCU (Micro Processor Unit), DC-to-DC regulators, digital audio I2S interface and I2C control interface, and SPI interface into a single chip.

The ALC4050 connects codecs and DACs that typically have digital I2S and are configured by an I2C interface to a USB host system with programmable capabilities in order to remove the need for complex audio configuration and operations. The ALC4050 integrates an S/PDIF output interface for external compressed audio data decoding.

The ALC4050 Universal Audio Jack, where it not only operates with OMTP and CTIA Headsets, but also as a Line-in/Microphone. The ALC4050 detects OMTP and CTIA headsets with no extra MOSFET or analog switch required. The ALC4050 provides a ‘Headset Push-Button Control’ function; certain types of push button behavior on the headset line can be detected, and control corresponding to individual push button behavior can be customized by the Realtek Audio FW according to customer’s requests.

2. Features

2.1. General Hardware Features

- Digital-to-Analog Converter with 100dBA SNR
- Analog-to-Digital Converter with 94dBA SNR
- One stereo DAC supports 8K/16K/22.05K/24K/32K/44.1K/48K/96K/176.4K/192K/384KHz Sample Rate, 16/24/32-bit resolution
- Two stereo ADCs support 8K/16K/22.05K/24K/32K/44.1K/48K/96K/176.4K/192K/384KHz Sample Rate, 16/24/32-bit resolution
- 2nd Gen. Realtek Proprietary Hardware Feed-Forward or Feedback Active Noise Cancellation (ANC)
- Integrates hardware Direct-Stream-Digital (DSD) native decoder (64Fs/128Fs/256Fs) and DSD over PCM (DoP) decoder and encoder (64Fs/128Fs) for both I2S and headphone outputs
- Class-G type amplifier for headphone output without DC blocking capacitors
- 9-Band hardware EQ function (HPFx1, BPFx4, LBFx1, Biquadx3) and AGC (Auto Gain Control) function for playback path
- 6-Band hardware EQ function for recording path (LPFx1, HPFx1, BPFx4)
- Microphone input Automatic Gain Control (AGC) function
- 0.5mA current consumption for USB suspend and Ultra-Low-Power for headphone playback
- One S/PDIF Out interface supports 44.1/48/88.2/96/176.4/192KHz sample rate for PCM format playback and AC-3 format data transfer
- Single-ended analog microphone inputs with volume gain control in 0.375dB per step
- Microphone boost gain settings of 0/10/20/30dB
- Low noise microphone and programmable MICBIAS voltage level
- Analog-to-analog pass-through path with volume gain adjustments
- Audio jack detection feature
- Supports combo jack with stereo headphone output and mono microphone input on a four-conductor headset jack for CTIA and OMTP type headsets without external components

- 4-Button Headset in-line controls support Android Wired Audio Headset Specification with customizable multi-function
- External active speaker humming noise cancellation
- One I2S interface supports 8K/16K/22.05K/32K/44.1K/48K/88.2K/96K/176.4K/192K/384kHz sample rate and , 16/24/32-bit resolution
- I2S digital interface supports TDM format up to 8CH output/input data transfer simultaneously
- I2C control interface supports master mode and slave mode
- Two stereo digital microphone interfaces with shared clock rate support 0.1875M/0.375M/0.75M/1.5M/3M/6MHz
- SPI (Serial Peripheral Interface, Mode 0~Mode 3) connection to serial flash for switching code and configuration of customized parameters
- UART interface for external devices
- Embedded 64K Byte flash and 16K Byte OTP for F/W programming
- Built-in Analog LDO, supports voltage input supply range from 3.0V to 5.0V
- 48-pin QFN 'Green' package

2.2. USB Controller Features

- Compliant with USB Specification 2.0 Full-Speed and High-Speed transfer mode
- Compliant with USB Audio Class Specification Rev1.0 and 2.0
- Supports 6 isochronous customizable endpoints for maximum 10 channel streaming, 3 UAC In and 3 UAC Out simultaneously
- ISO In/Out endpoints support customizable channel configuration for 1/2/3/4/5/6/8 channel mappings
- Supports one endpoint for control transfer and two endpoints for interrupt transfer
- Supports Selective Suspend mode
- Supports USB LPM-L1 protocol
- Supports jack detection, headset's in-line button, and GPIOs Remote wakeup function in suspend mode

- Internal PLL supports non-crystal design
- Built-in Self-Loop-Back BIST for testing purposes

2.3. Micro Controller Unit

- On-chip high-performance and low-power MCU
- Software controlled connection to USB bus for re-enumeration
- Internal programmable memory support for various Realtek codec and audio configurations
- Watchdog control for MCU reset and interrupt
- Configurable VID (Vendor ID), PID (Product ID), and serial number string

2.4. Configurable GPIO Pins

- Programmable inputs and outputs for control purposes
- Toggle PWM LED driver and controller upon firmware or custom driver customizations

2.5. Software Features

- Does not require a custom audio driver
- USB Audio Class compliant; operates with native driver in Microsoft Windows XP, VISTA, Windows 7, Windows 8, Windows 8.1, and Windows 10
- Realtek custom audio driver provides a certified logo driver for Microsoft Windows XP, VISTA, Windows 7, Windows 8, Windows 8.1, and Windows 10
- Realtek Control Panel (Realtek Audio Manager) for enhanced user experience
  - Audio I/O Jack and Device settings and controls
  - Application Enhancements for both voice processing and audio post processing and effects
  - Reduces audio software development and usage complexity
- Selective suspend function saves power in Standby mode

3. System Applications

- USB Docking Station for Notebook, Tablet, PCs
- Mobile Phone audio accessary
- Embedded USB audio applications
- USB Type-C audio headset, microphone, speaker and generic audio accessories
- USB gaming headset and generic audio accessories

4. Block Diagram

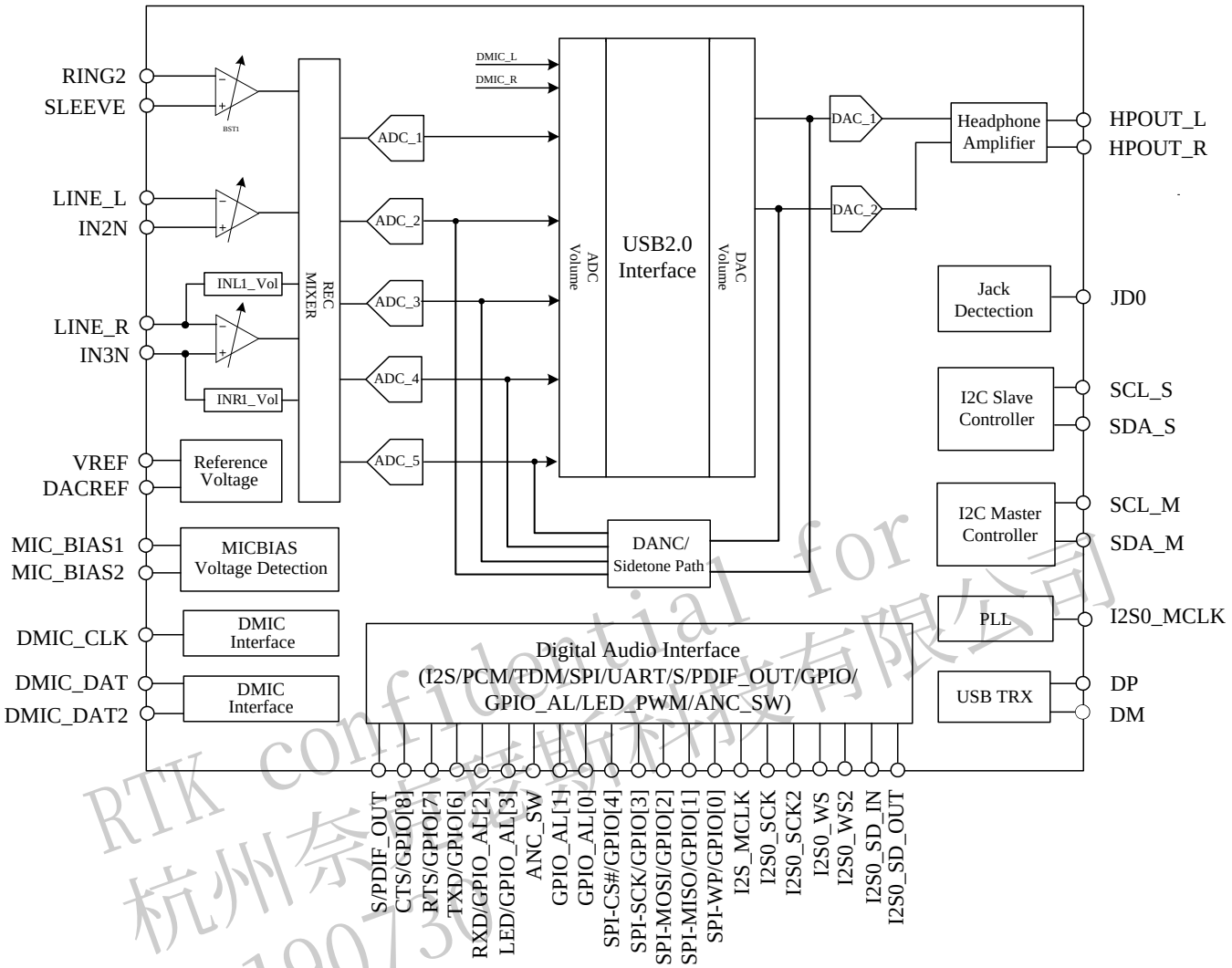


Figure 1. Block Diagram

5. Pin Assignments

5.1. Pin Assignments Figure

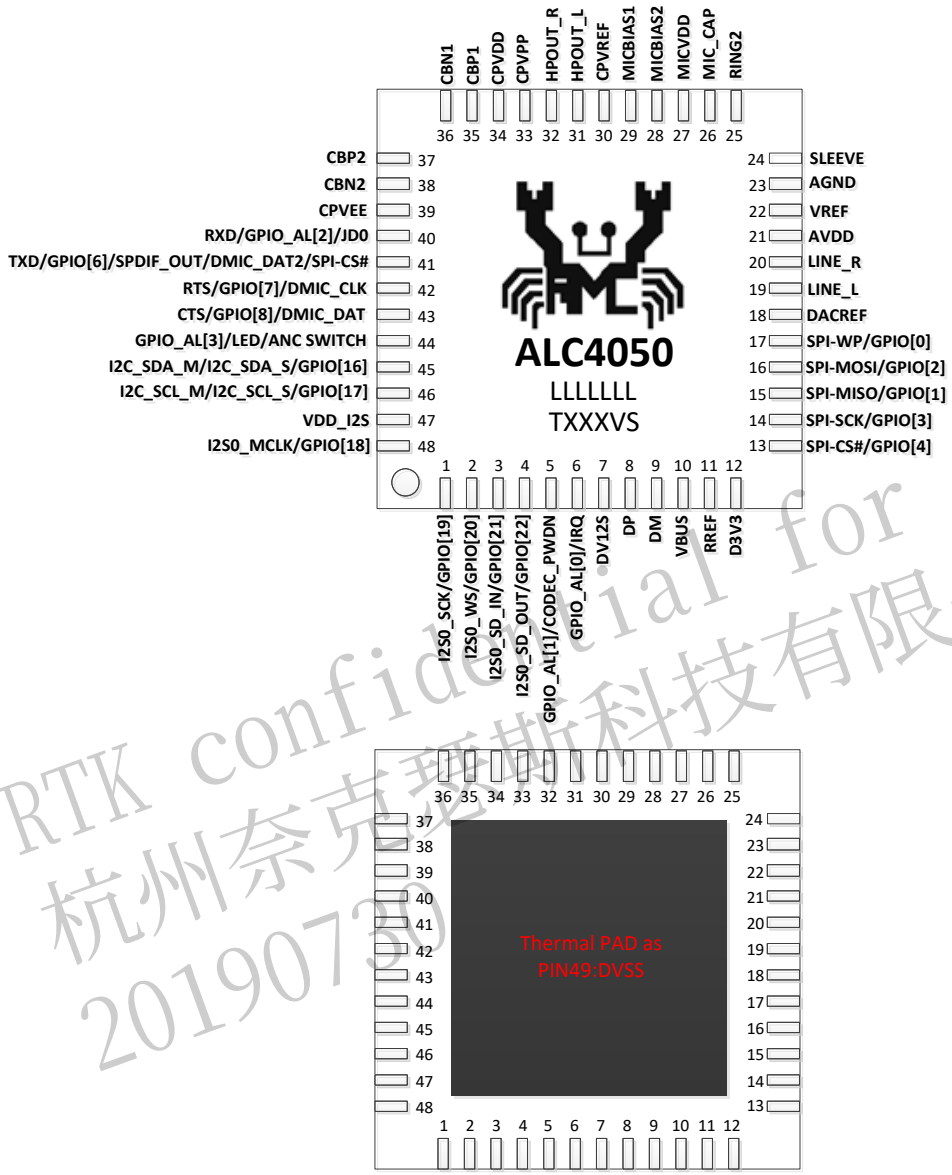


Figure 2. Pin Assignments

5.2. Package and Version Identification

Green package is indicated by a ‘G’ in the location marked ‘T’ in ‘TXXXVS’ in Figure 2.

6. Pin Descriptions

6.1. I/O Type Description

Table 1. I/O Type Description

I/O Type	Description
I	Input
O	Output
IH	Input with internal pull-up 200K
IL	Input with internal pull-down 200K
IO	Input/Output
IOH	Input/Output with internal pull-up 200K
IOL	Input/Output with internal pull-down 200K
IOSH	Input/Output with Schmitt trigger
IO-U	USB related IO
CLK	Clock related IO
PWR-O	Power output pin
PWR-I	Power input pin
GND	Ground related pin

6.2. USB Transceiver Interface

Table 2. USB Transceiver Interface

Name	Type	Pin No.	Description
DP	IO-U	8	USB D+ signal
DM	IO-U	9	USB D- signal
RREF	-	11	External Reference. Requires 1% precision 6.25k or 6.2k resistor to ground
-			Total: 3 Pins

6.3. GPIO, UART, DMIC, and SPI Interface

Table 3. GPIO, UART, DMIC, and SPI Interface

Name	Type	Pin No.	Description
GPIO_AL[1] /Codec_PWDN	IOH	5	General purpose input and output; operates even in USB suspend mode
GPIO_AL[0] /IRQ	IOH	6	General purpose input and output; operates even in USB suspend mode
SPI-WP# /GPIO[0]	IOH	17	SPI serial flash write protected /General purpose input and output
SPI-MOSI /GPIO[2]	IOH	16	SPI serial data in /General purpose input and output
SPI-MISO /GPIO[1]	IOH	15	SPI serial data out /General purpose input and output
SPI-SCK /GPIO[3]	IOH	14	SPI clock signal /General purpose input and output
SPI-CS# /GPIO[4]	IOH	13	SPI chip select /General purpose input and output
GPIO_AL[3] /LED	IOH	44	General purpose input and output; operates even in USB suspend mode /LED controller
CTS /GPIO[8] /DMIC_DAT	IOH	43	Clear-to-send handshaking signal /General purpose input and output /Primary DMIC data
RTS /GPIO[7] /DMIC_CLK	IOH	42	Request-to-send handshaking signal /General purpose input and output /DMIC clock
TXD /GPIO[6] /SPDIF_OUT /DMIC_DAT2 /SPI-CS#	IOH	41	Serial data transmit /General purpose input and output /SPDIF-Out /Secondary DMIC data /SPI chip select
RXD /GPIO_AL[2] /JD0	IOH	40	Serial data receive /General purpose input and output /Jack detection
-			Total: 12 Pins

6.4. I2C Interface

Table 4. I2C Interface

Name	Type	Pin No.	Description
I2C_SDA_M /I2C_SDA_S /GPIO[16]	IO	45	I2C Bus Data – Master /I2C Bus Data – Slave /General purpose input and output
I2C_SCL_M /I2C_SCL_S /GPIO[17]	IO	46	I2C Bus clock– Master /I2C Bus clock – Slave /General purpose input and output
-			Total: 2 Pins

6.5. I2S Interface

Table 5. I2S Interface

Name	Type	Pin No.	Description
I2S0_SCK /GPIO[19]	IO	1	I2S Clock output /General purpose input and output
I2S0_WS /GPIO[20]	IO	2	I2S channel select /General purpose input and output
I2S0_SD_IN /GPIO[21]	IO	3	I2S data input /General purpose input and output
I2S0_SD_OUT /GPIO[22]	IO	4	I2S data output /General purpose input and output
I2S0_MCLK /GPIO[18]	IO	48	System Master Clock /General purpose input and output
-			Total: 5 Pins

6.6. Analog I/O

Table 6. Analog I/O

Name	Type	Pin No.	Description	Characteristic Definition
RING2	I	25	Combo jack microphone input	Analog input
SLEEVE	I	24	Combo jack microphone input	Analog input
LINE_L	I	19	Line input left channel	Analog input
LINE_R	I	20	Line input right channel	Analog input
HPOUT_R	O	32	Headphone output Right channel	Analog output
HPOUT_L	O	31	Headphone output Left channel	Analog output
-			Total: 6 Pins	

6.7. Filter/Reference

Table 7. Filter/Reference

Name	Type	Pin No.	Description	Characteristic Definition
VREF	R	22	Analog I/O reference voltage	Capacitor to analog ground
CPVREF	R	30	Analog I/O reference voltage	To analog ground
MICBIAS1	O	29	MIC BIAS Voltage output	Programmable Analog DC output
MICBIAS2	O	28	MIC BIAS Voltage output	Programmable Analog DC output
MIC_CAP	I	26	Microphone input reference voltage	Capacitor to analog ground
DACREF	O	18	DAC/ADC reference voltage	Capacitor to analog ground
CBN1	R	36	Charge pump Bucket Capacitor	2.2µF capacitor to CPN1
CBP1	R	35	Charge pump Bucket Capacitor	2.2µF capacitor to CPP1
CBN2	R	38	Charge pump Bucket Capacitor	2.2µF capacitor to CPN2
CBP2	R	37	Charge pump Bucket Capacitor	2.2µF capacitor to CPP2
-			Total: 10 Pins	

6.8. Power/Ground

Table 8. Power/Ground

Name	Type	Pin No.	Description
DV12S	PWR-O	7	Regulated 1.2V output for core power
D3V3	PWR-O	12	3.3V power output from integrated VBUS-to-3.3V regulator and I/O interface
VBUS	PWR-I	10	USB bus 5.0V power input for integrated multiple regulators. This power pin can accept 3.3V of USB power input for 3.3V system
VDD_I2S	PWR-O	47	VDD_I2S for companion I2S IO power
AVDD	PWR-O	21	Analog power
CPVPP	PWR-O	33	Charge Pump Positive Voltage Output
CPVDD	PWR-O	34	Charge Pump Voltage Output
CPVEE	PWR-O	39	Charge Pump Negative Voltage Output
MICVDD	PWR-O	27	Microphone bias power
AGND	GND	23	Analog ground
Thermal Pad	GND	49	DVSS/Power Stage Ground
-			Total: 11 Pins

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Table 9. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies Digital Power	VBus	-0.3	5.0	5.5	V
Ambient Operating Temperature	Ta	0	-	+70	^{o}C
Storage Temperature	Ts	-40	-	+125	^{o}C
ESD (Electrostatic Discharge)					
-	Susceptibility Voltage				
All Pins	Pass 3500V				

7.2. Recommended Operating Condition

Table 10. Recommended Operating Condition

Symbol	Description	Min.	Typ.	Max.	Unit
VBus	Supply Voltage	3.3	5	5.5	V

7.3. DC Characteristics

Table 11. DC Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
V_{IH}	Input Voltage High	2	-	3.3	V
V_{IL}	Input Voltage Low	-0.5	-	0.8	V
V_{OH}	Output Voltage High	2.4	-	-	V
V_{OL}	Output Voltage Low	-	-	0.4	V
I_{OH}	Output Current High	-	-	4	mA
I_{OL}	Output Current Low	-	-	4	mA

7.4. AC Characteristics

7.4.1. SPDIF Output Timing

Table 12. SPDIF Output Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
SPDIF-OUT Frequency	-	-	3.072	-	MHz
SPDIF-OUT Period	Tcycle	-	325.6	-	ns
SPDIF-OUT Jitter	Tjitter	-	-	4	ns
SPDIF-OUT High Level Width	THigh	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
SPDIF-OUT Low Level Width	TLow	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
SPDIF-OUT Rising Time	Trise	-	2.0	-	ns
SPDIF-OUT Falling Time	Tfall	-	2.0	-	ns

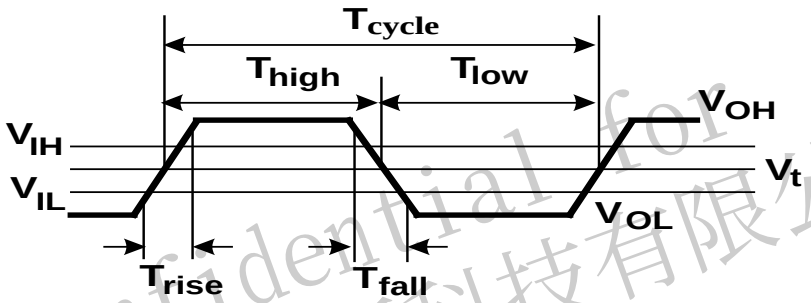


Figure 3. SPDIF Output Timing

7.4.2. I2C Control Interface

Table 13. I2C Control Interface

Parameter	Symbol	Min	Typ	Max	Units
Clock Low Pulse Duration	Tw(9)	1.3	-	-	µs
Clock High Pulse Duration	Tw(10)	0.6	-	-	µs
Clock Frequency	f	0	-	400(*2)	KHz
Setup Time for a Repeated START Condition	Tsu(6)	600	-	-	ns
Start Hold Time	Th(5)	600	-	-	ns
Data Setup Time	Tsu(7)	100	-	-	ns
Data Hold Time	Th(6)	-	-	900	ns
Rising Time	Tr	-	-	300	ns
Falling Time	Tf	-	-	300	ns
Setup Time	Tsu(8)	600	-	-	ns
Bus Free Time Between a STOP and START Condition	Tbuf	1.3	-	-	µs
Pulse Width of Spikes Suppressed Input Filter	Tsp	0	-	50	ns

Note 1: The host must apply the MCLK clock during I2C control interface access.
*Note 2: If MCLK provides 256*8KHz, I2C clock frequency only can support 400 KHz*
Note 3: There is no need for MCLK in I2C communications.

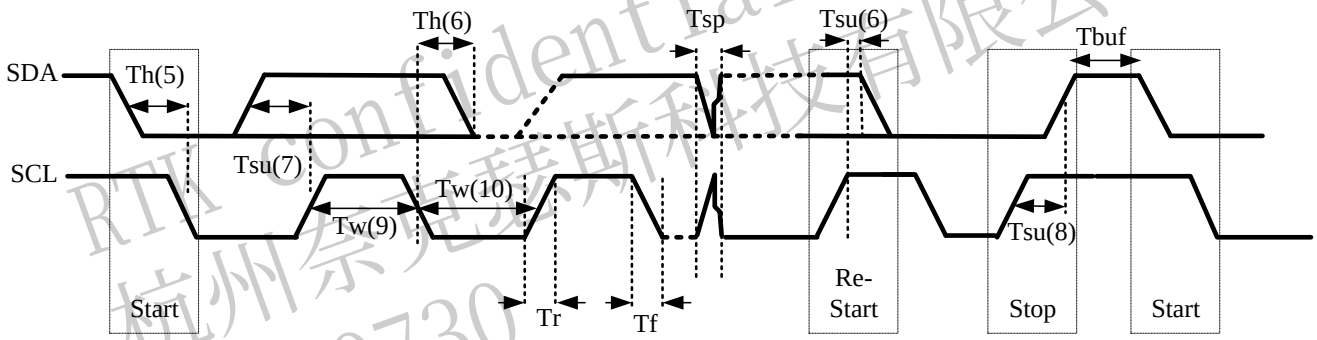


Figure 4. I2C Control Interface

7.4.3. I2S Master Mode

Table 14. I2S Master Mode

Parameter	Symbol	Min	Typ	Max	Units
LRCK output to BCLK delay	t_{LRD}	-	-	30	ns
Data output to BCLK delay	t_{ADD}	-	-	30	ns
Data input Setup time	t_{DAS}	10	-	-	ns
Data input Hold time	t_{DAH}	10	-	-	ns

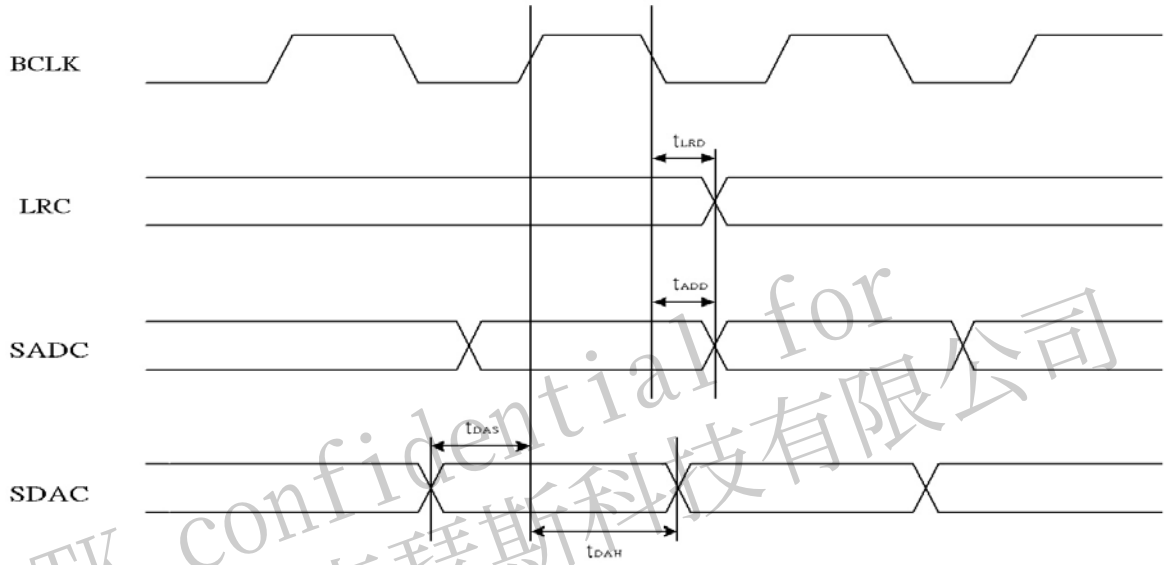


Figure 5. I2S Master Mode Timing

7.5. Analog Performance

Standard Test Conditions

- Tambient=25°C, VBUS=5.0V ±5%
- 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms
- 10KΩ/50pF load; Test bench Characterization BW: 20Hz~22kHz

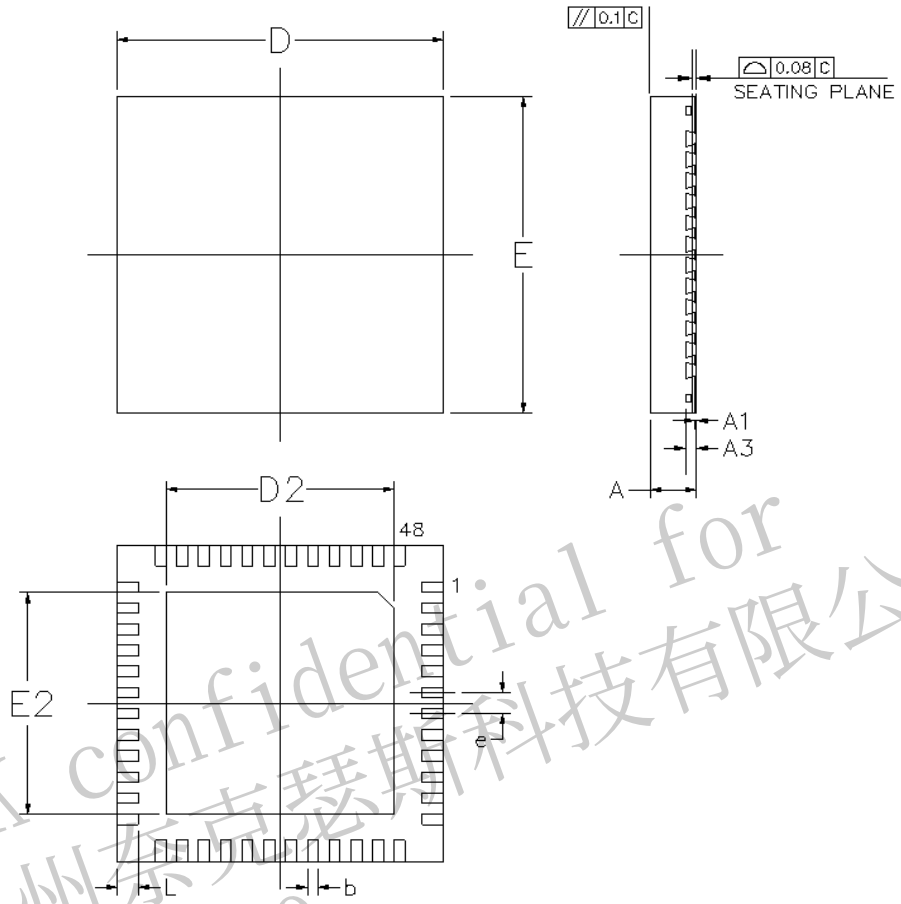
Table 15. Analog Performance

Parameter	Min	Typ	Max	Units
Full-Scale Input Voltage				
All ADC (Gain=0dB)	-	0.6	-	Vrms
Line Input	-	0.6	-	
MIC Input	-	0.6	-	
Full-Scale Output Voltage				
All DAC (Gain=0dB)	-	1.0	-	Vrms
Headphone Out @10KΩ load	-	1.0	-	
Headphone Out @32Ω load	-	1.0	-	
Headphone Out @16Ω Load	-	0.9	-	
SNR (A Weighted)				
ADC	-	94	-	dB FSA
DAC	-	100	-	
Headphone Out @16Ω Load	-	98	-	
Headphone Out @32Ω Load	-	98	-	
MIC_IN to Stereo ADC with 0dB	-	93	-	
LINE_IN to stereo ADC with 0dB	-	93	-	
Total Harmonic Distortion Plus Noise, THD+N				
ADC	-	-84	-	dB FS
DAC	-	-85	-	
Headphone Out @16Ω Load	-	-81	-	
Headphone Out @32Ω Load	-	-81	-	
Frequency Response				
ADC (-3dB lower edge, -1dB higher edge)	10	-	0.454*Fs	Hz
DAC (-3dB lower edge, -1dB higher edge)	10	-	0.454*Fs	
Crosstalk	-	-80	-	dB
Current consumption @ Idle(HID only)	-	14	-	mA
Current consumption @ Idle(DAC+ADC)	-	24.5	-	mA
Current consumption @ Active	-	27.5	-	mA
Current consumption @ Suspend	-	495	-	µA

Note: FSA=Full-Scale with A-weighting filter. FS=Full-Scale.

8. Mechanical Dimensions

8.1. Mechanical Dimensions – QFN 48 6x6mm Outline



8.2. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	6.00BSC			0.236BSC		
D2/E2	4.15	4.4	4.65	0.163	0.173	0.183
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes: CONTROLLING DIMENSION: MILLIMETER (mm).
REFERENCE DOCUMENT: JEDEC MO-220

9. Application Circuits

To guarantee the best compatibility and performance quality in hardware design with specific requirements, please contact Realtek to receive the latest application circuits. Any modification made to the reference circuits is recommended to be reviewed by Realtek. Realtek may update the latest application circuits without modifying this datasheet.

10. Ordering Information

Table 16. Ordering Information

Part Number	Package	Status
ALC4050-VA1-CG	MQFN-48 'Green' Package (6mm x 6mm)	MP

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