Version : 1.3

TECHNICAL SPECIFICATION

MODEL NO. : PA035XSE

☐Customer's Approved

Customer _____

Date _____

By _____

☐PVI's Confirmation

Approved By _____

Prepared By _____

FOR MORE INFORMATION:
AZ DISPLAYS, INC.
75 COLUMBIA, ALISO VIEJO, CA, 92656
Http://www.AZDISPLAYS.com

Date : Jan.20,2005

This technical specification is subject to change without notice.
Please return 1 copy with your signature on this page for approval.

TECHNICAL SPECIFICATION

CONTENTS

1. Application

This technical specification applies to 3.5" color TFT-LCD panel. The 3.5" color TFT LCD panel is designed for camcorder, digital camera application and other electronic products which require high quality flat panel displays.

2. Features

. Compatible with NTSC or PAL system

. High Resolution：224,640 Dots

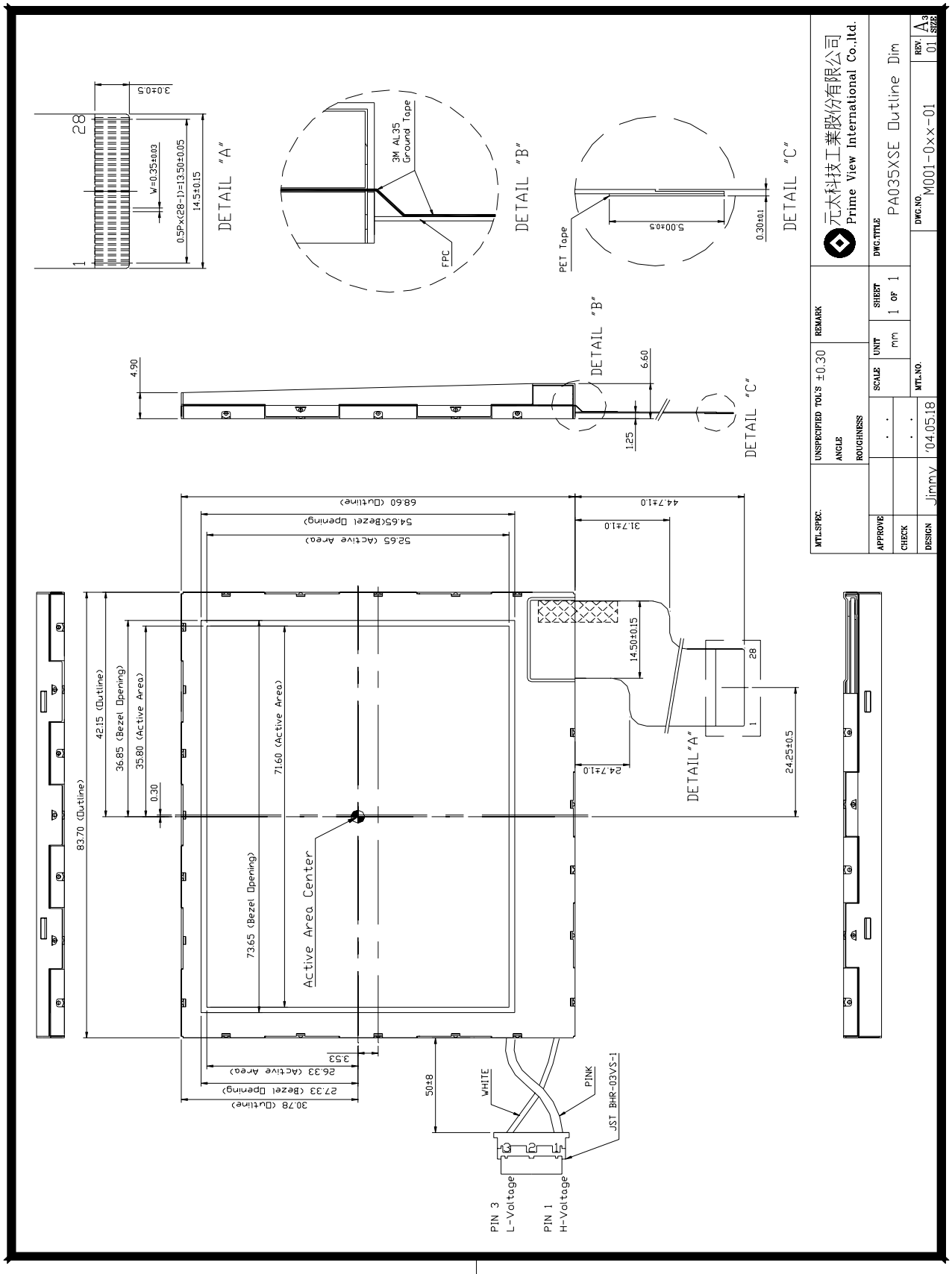
. Optimum Viewing Direction： 6 o'clock

. Up/Down and Left/Right Image Reversion

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	3.5 (diagonal)	inch
Surface Treatment	Anti-Glare	
Display Format	960×234	dot
Active Area	71.6×52.65	mm
Dot Pitch	0.0745 (H)×0.225 (V)	mm
Pixel Configuration	Delta	
Outline Dimension	83.7(W)×68.6(H)×6.6 (D)	mm
Weight	58±5	g

4. Mechanical Drawing of panel:



5. Input / Output Terminals

Pin No	Symbol	I/O	Description	Remark
1	STH1	I/O	Start pulse for source driver	Note 5-1
2	AV_{SS}	I	Analog GND for source driver	
3	AV_{DD}	I	Analog power input for source driver	Note 5-2
4	V_B	I	Video Input B	Note 5-4
5	V_G	I	Video Input G	
6	V_R	I	Video Input R	
7	V_{SS}	I	Digital GND	
8	V_{DD}	I	Digital power input	Note 5-3
9	CPH1	I	Sampling and shift clock for source driver	
10	CPH2	I	Sampling and shift clock for source driver	
11	CPH3	I	Sampling and shift clock for source driver	
12	STH2	I/O	Start pulse for source driver	Note 5-1
13	Q2H	I	Video input rotation control	
14	INH	I	Output enable for source driver	
15	R/L	I	Left/Right Control for source driver	Note 5-1
16	V_{COM}	I	Common electrode voltage	Note 5-4
17	V_{COM}	I	Common electrode voltage	
18	XOE	I	Output enable for gate driver	
19	CPV	I	Clock input for gate driver	
20	U/D	I	Up/Down Control for gate driver	
21	DIO2	I/O	Vertical start pulse	Note 5-5
22	DIO1	I/O	Vertical start pulse	
23	V_{GL}	I	Gate off voltage(alternative every 1-H)	Note 5-4
24	V_{EE}	I	Gate driver negative voltage	Note 5-6
25	V_{SS}	I	GND	
26	V_{CC}	I	Logic power for gate driver	Note 5-3
27	V_{GH}	I	Gate on voltage	Note 5-7
28	GND	-	B/L case GND	-

Note 5-1：STH1, STH2 and R/L mode

R/L	STH1	STH2	Remark
High(VDD)	Input	Output	Left to Right
Low(0 Volt.)	Output	Input	Right to Left

Note 5-2：AV_{DD} = +5V (Typ.)

Note 5-3：V_{DD}, V_{CC} = +3.3V (Typ.)

Note 5-4：V_{COM} = $6V_{PP}$.

Phase of the video signal input and V_{COM}
The relation between these values could refer to 8-1 Operating condition.

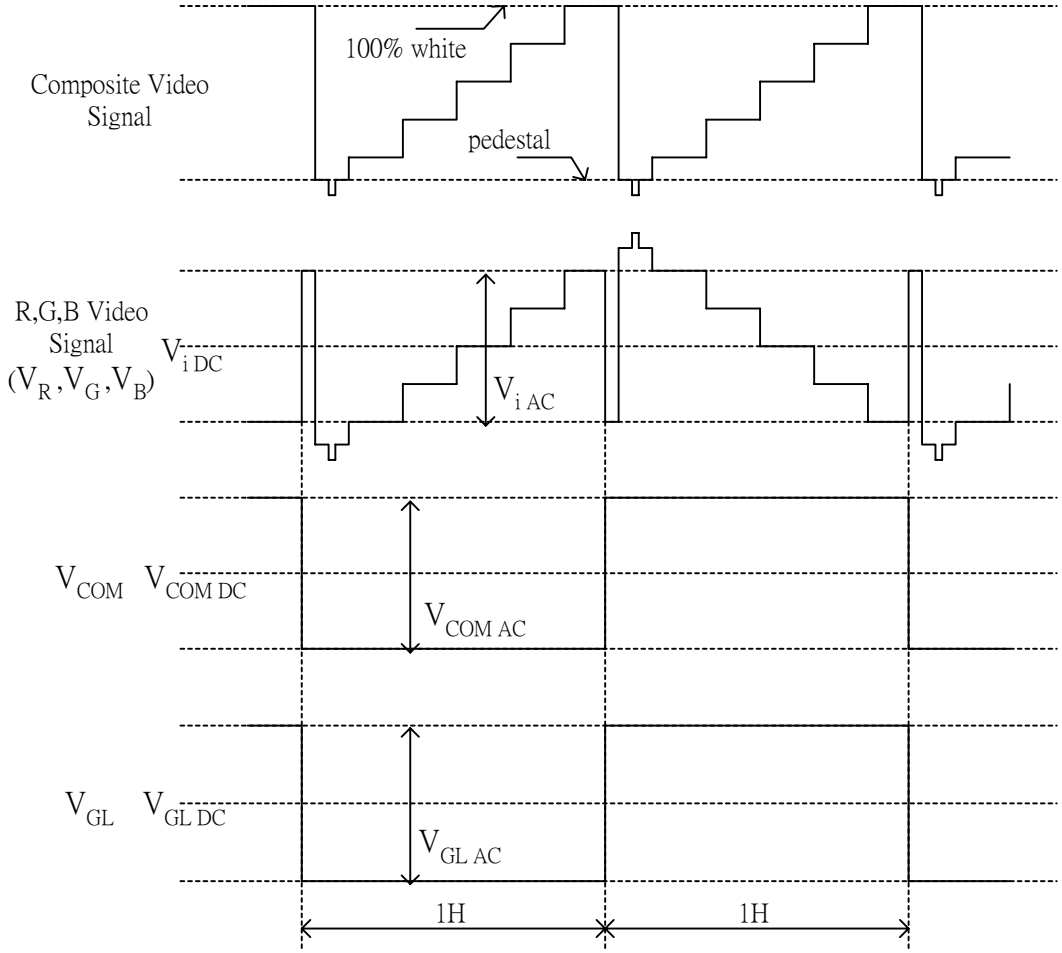


Fig.1

Liquid crystal transmission of the video signal input, V_{COM} and timing

	V_{COM}	
	H Level	L Level
Video Signal Input Maximum	Black	White
Video Signal Input Minimum	White	Black

White : maximum transmission / Black : minimum transmission

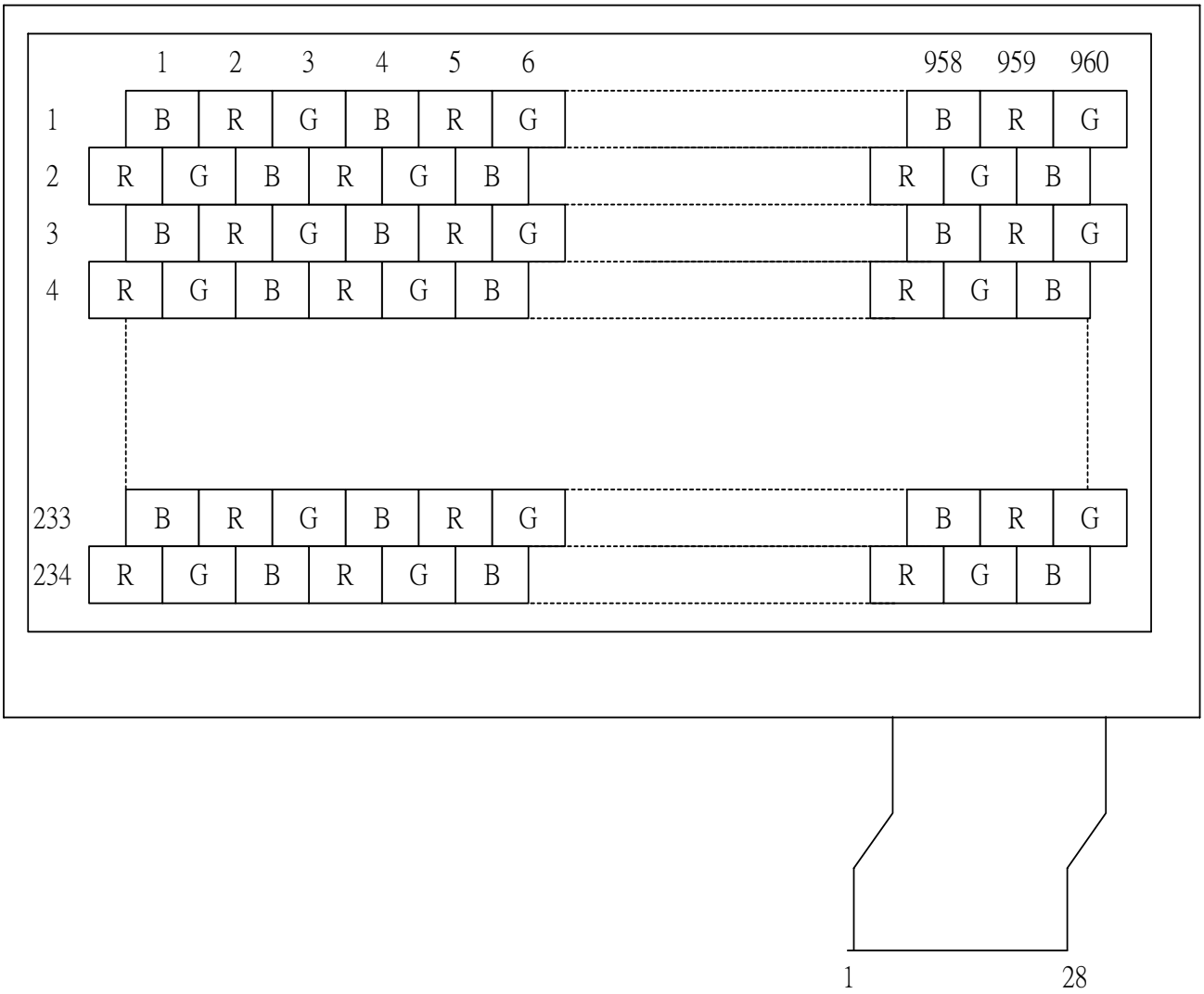
Note 5-5：DIO1, DIO2 and U/D mode

U/D	DIO1	DIO2	Remark
High (VDD)	Input	Output	Down to Up
Low (0 Volt.)	Output	Input	Up to Down

Note 5-6：V_{EE} = -15V (Typ.).

Note 5-7：V_{GH} = +17V (Typ.).

6. Pixel Arrangement and input connector pin NO.



7. Absolute Maximum Ratings:
The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

GND = 0 V， Ta = 25 ℃

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage for Source Driver	Analog	AV_{DD}	-0.3	+7.0		
	Digital	V_{DD}	-0.3	+7.0		
Supply Voltage for Gate Driver	Positive	V_{GH}	-0.3	+45	V	
	Negative	V_{GL}	-23	+0.3	V	
		V_{GH}-V_{GL}	+15	+40	V	
Analog input voltage		V_{Video}	-0.3	+7.3	V	Notes:7-1
Storage Temperature			-20	+70	℃	
Operation Temperature			0	+60	℃	Notes:7-2

Notes 7-1 : Analog Input Voltage means V_R,V_G,V_B.

Notes 7-2 : Operating Temperature define that contrast, response time, other display optical character are Ta=+25.

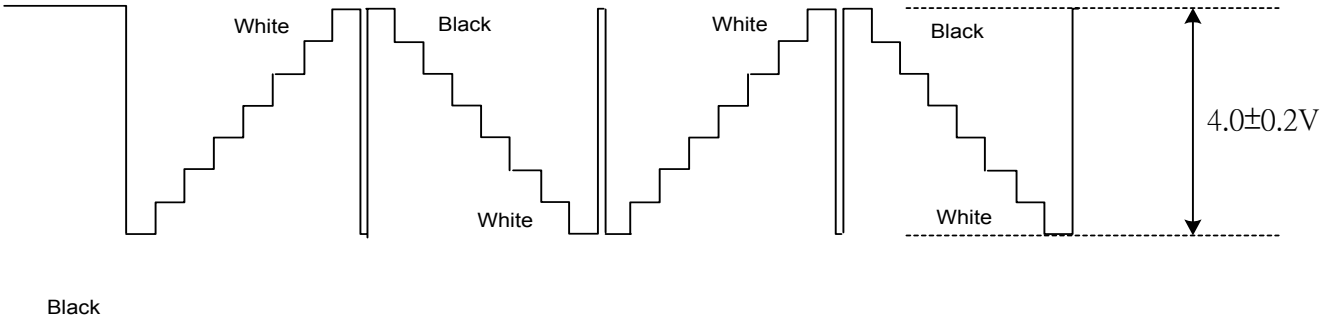
8. Electrical Characteristics

8-1) Operating Condition

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply		V_{CC} V_{DD}	+3.0	+3.3	+3.6	V	
		AV_{DD}	+4.5	+5.0	+5.5	V	
		V_{GH}	+15.0	+17.0	+19.0	V	
		V_{EE}	-15.5	-15.0	-14.5	V	
		$V_{GL\ AC}$	-	+6.0	-	V_{P-P}	AC Component of V_{GL}
		$V_{GL\ DC}$	-12.5	-11.0	-9.5	V	DC Component of V_{GL}
Video Signal (V_R, V_G, V_B)		$V_{i\ AC}$	-	+4.0	+4.2	V_{P-P}	AC Component Note 8-2
		$V_{i\ DC}$	-	+2.5	-	V	DC Component
V_{COM}		$V_{COM\ AC}$	-	+6.0	-	V_{P-P}	AC Component of V_{COM}
		$V_{COM\ DC}$	0.76	0.96	11.6	V	DC Component of V_{COM}
	H Level	+0.7 V_{DD}	-	-	-	V	Note 8-1
	L Level	-	-	+0.3 V_{DD}	+0.3 V_{DD}	V	

Note 8-1：STH1,STH2,CPH1,CPH2,CPH3,Q2H,INH,CPV,XOE,DIO1,DIO2

Note 8-2：Both NTSC and PAL system Video Signal input waveform is based on 8 steps gray scale.



8-2)Current Consumption (GND=AV_{SS}=0V)

Ta= 25 ℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Current for Driver	I_{GH}	V_{GH}=+17V	-	0.055	0.083	mA	
	I_{GL}	V_{GL}=-12V	-	0.067	0.087	mA	V_{GL} center voltage
	I_{CC}	V_{CC}=+3.3V	-	0.441	0.563	mA	
	AI_{DD}	AV_{DD}=+5V	-	7	10	mA	
	I_{DD}	V_{DD}=+3.3V	-	1.2	3	mA	
	I_{EE}	V_{EE}=-15V	-	0.441	0.600	mA	

8-3) Backlight driving & Power Consumption

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
3	VL2	Input terminal (Low voltage side)	Note 8-3

Note 8-3：Low voltage side of backlight inverter connects with Ground of inverter circuits.

Ta= 25 ℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	-	265	-	Vrms	I_L=3mA
Lamp current	I_L	2	3	5	mA	
Lamp frequency	P_L	25	35	65	KHz	Note 8-4
Kick-off voltage(25℃)	Vs	-	-	400	Vrms	Note 8-5
Kick-off voltage(0℃)	Vs	-	-	520	Vrms	

Note 8-4 : The waveform of lamp driving voltage should be as closed to a perfect SIN wave as possible.

Note 8-5 : This value is not output voltage of inverter.
The voltage of inverter must larger than the starting voltage.
The kick-off time must larger than 1 second.

8-4) Power Consumption

Ta= 25 ℃

Parameter	Symbol	Conditions	TYP.	Unit	Remark
LCD Panel Power Consumption			50	mW	Note 8-6
Backlight Lamp Power Consumption			0.65	W	Note 8-7
Total Power Consumption			0.69	W	

Note 8-6：The power consumption for backlight is not included.

Note 8-7：Backlight lamp power consumption is calculated by $I_L \times V_L$.

8-5) Input / Output Connector

1. LCD Module Connector
   FFC Down Connector,
   28 Pins
   Pitch：0.5 mm

B) Backlight Connector
   JST BHR-03VS-1
   Pin No.：3
   Pitch：4 mm

8-6) Timing Characteristics Of Input Signals

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
1Field Scanning Period	t1V	-	262.5	-	H	
1Line Scanning Period	t1H	-	63.5	-	μs	
Source Driver Operating Frequency	fhc	4	6.4	8	MHz	
Signal Sampling Pulse Width	tchw	125	156.25	250	ns	
Signal Sampling Pulse Delay	tchd	47.65	52	58.25	ns	tchd 12,23
Signal Sampling Pulse Width(H)	tchwh	71.45	78.12	87.35	ns	
Signal Sampling Pulse Delay(L)	tchwl	71.45	78.12	87.35	ns	
Source Start Signal Pulse Width	tshw	45	156.25	315	ns	*tshset=tshhld
Source Start Signal Setup Time	tshset	20	78.12	-	ns	
Source Start Signal Hold Time	tshhld	20	78.12	-	ns	
Source Output Enable Pulse Width	tohw	1.0		-	μs	
Source Start Signal Rising Time	tss	-	9.8	-	μs	
Video Input Signal Start Point	tvs	-	10.0	-	μs	
Phase Difference Between OEH&CPV	toc	1.5	2.3	-	μs	
Gate Clock Period	tcvw	10	63.5	-	μs	
Gate Clock Pulse Width(H)	tcvwh	10	31.7	48	μs	
Gate Clock Pulse Width(L)	tcvwl	10	31.7	48	μs	
Gate Start Signal Pulse Width	tsvw	5	63.5	126**	μs	**tsvset=tsvhld
Gate Start Signal Setup Time	tsvset	5	53.2	-	μs	
Gate Start Signal Hold Time	tsvhld	5	10.3	-	μs	
Phase Difference Between OEH&STH	tosp	-	4	-	μs	
Phase Difference Between SYNC&OEH	tohs	-	1.4	-	μs	
Gate Output Enable Pulse Width	toev	-	2.5	-	μs	
V_{COM} Delay Time	t_{DCOM}	-	-	3	μs	
RGB Delay Time	t_{DRGB}	-	-	2	μs	
Vertical Display Start	tsv	-	3	-	tH	

8-7) Signal Timing Waveforms

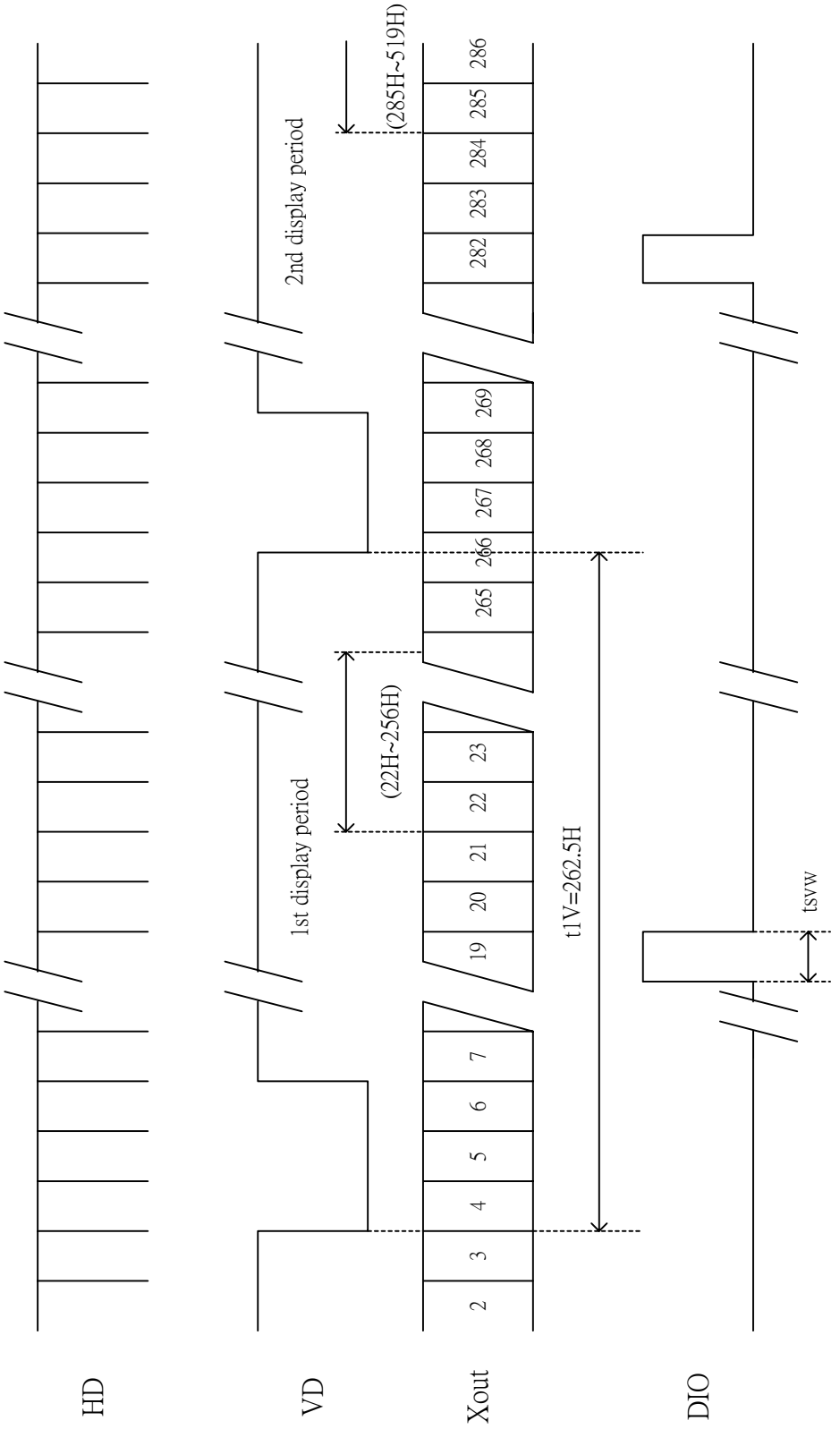
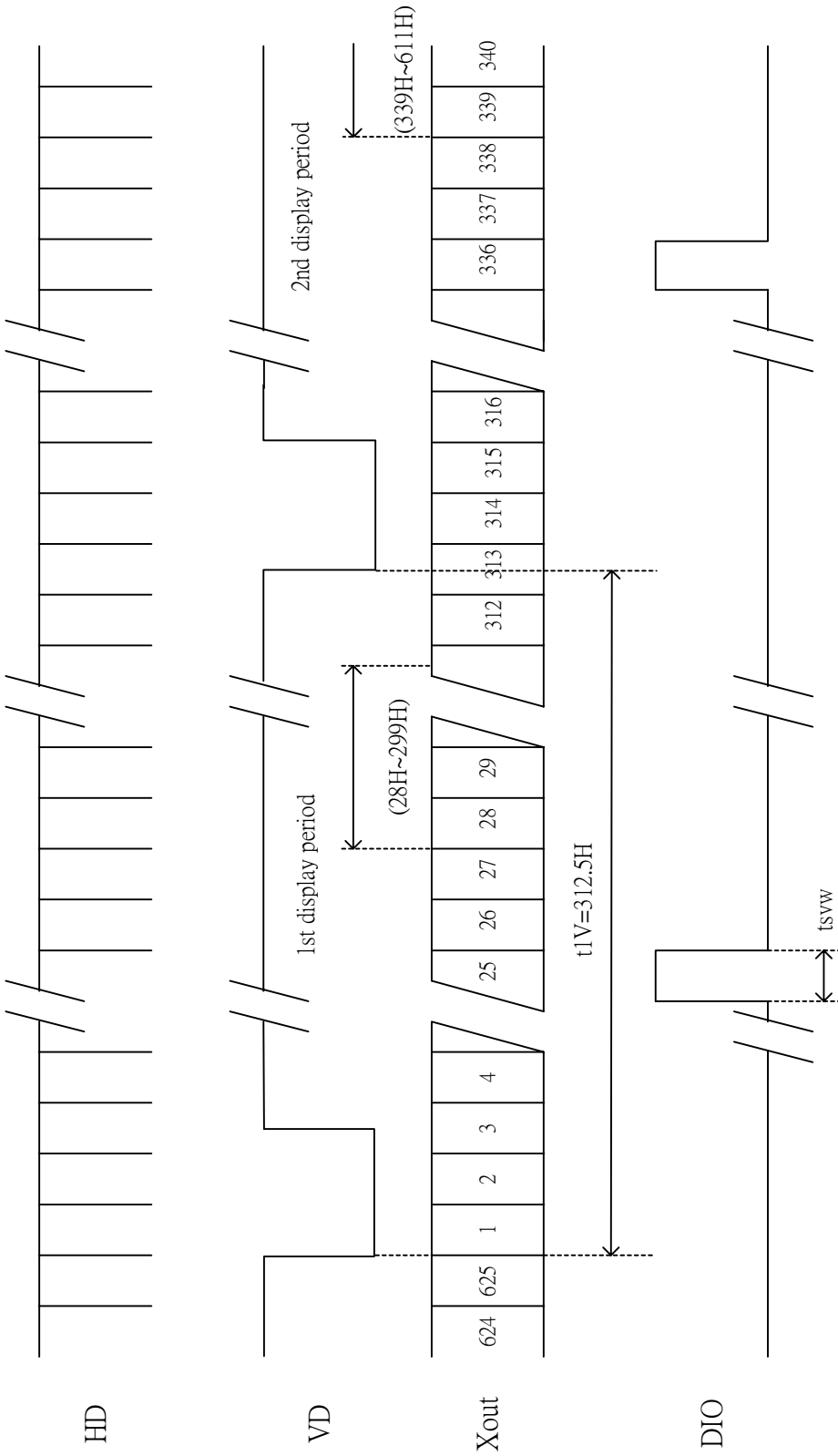


Fig. 8-1 Vertical Start Line for NTSC



** odd field : Scan lines 14n+6 14n+12 (n = 2, 3, 4..) are not displayed.
even field : Scan lines 14n+12 14n+20 (n = 2, 3, 4..) are not displayed.

Fig. 8-1 Vertical Start Line for PAL

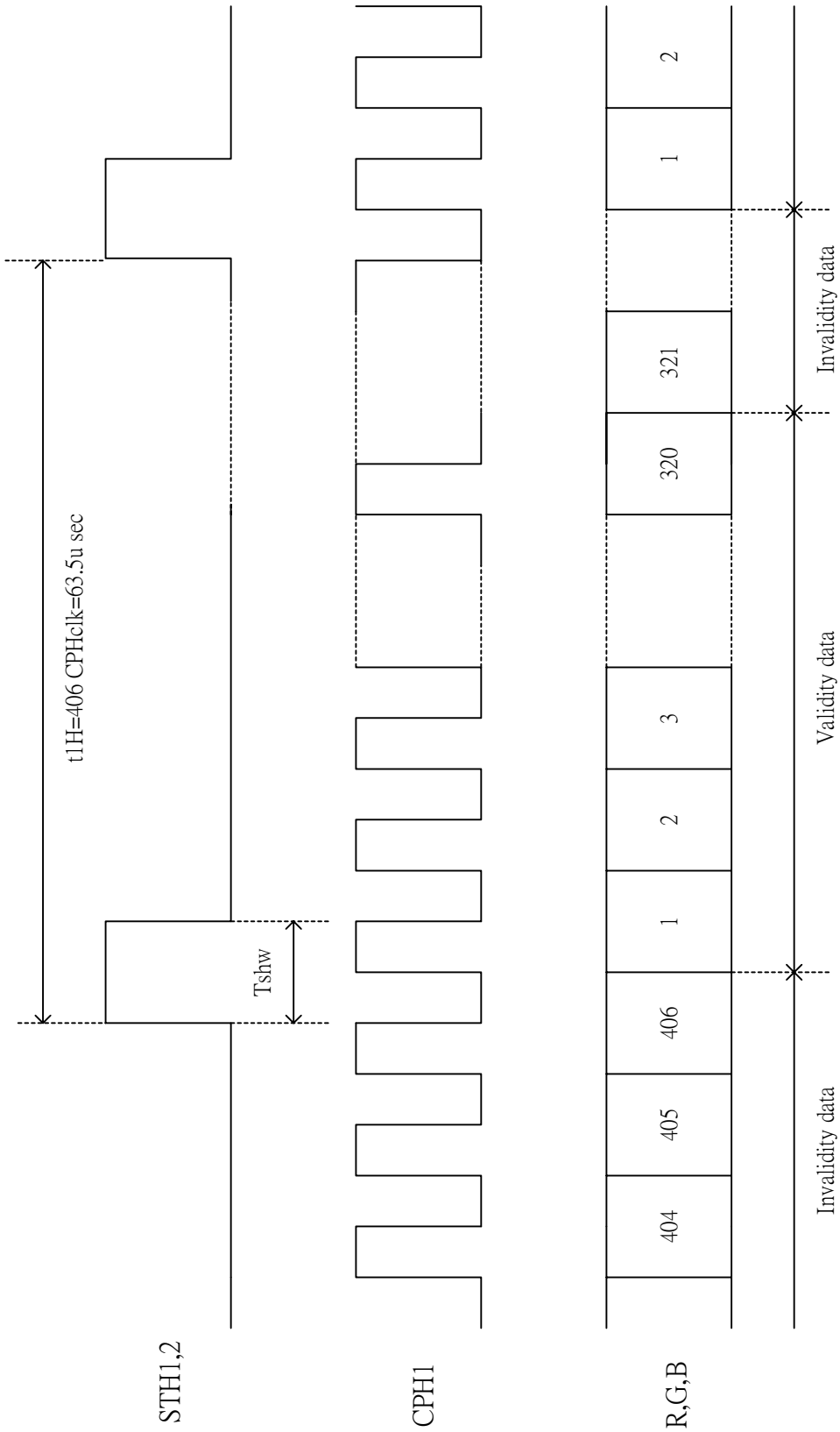


Fig. 8-2 Horizontal Start Pixel

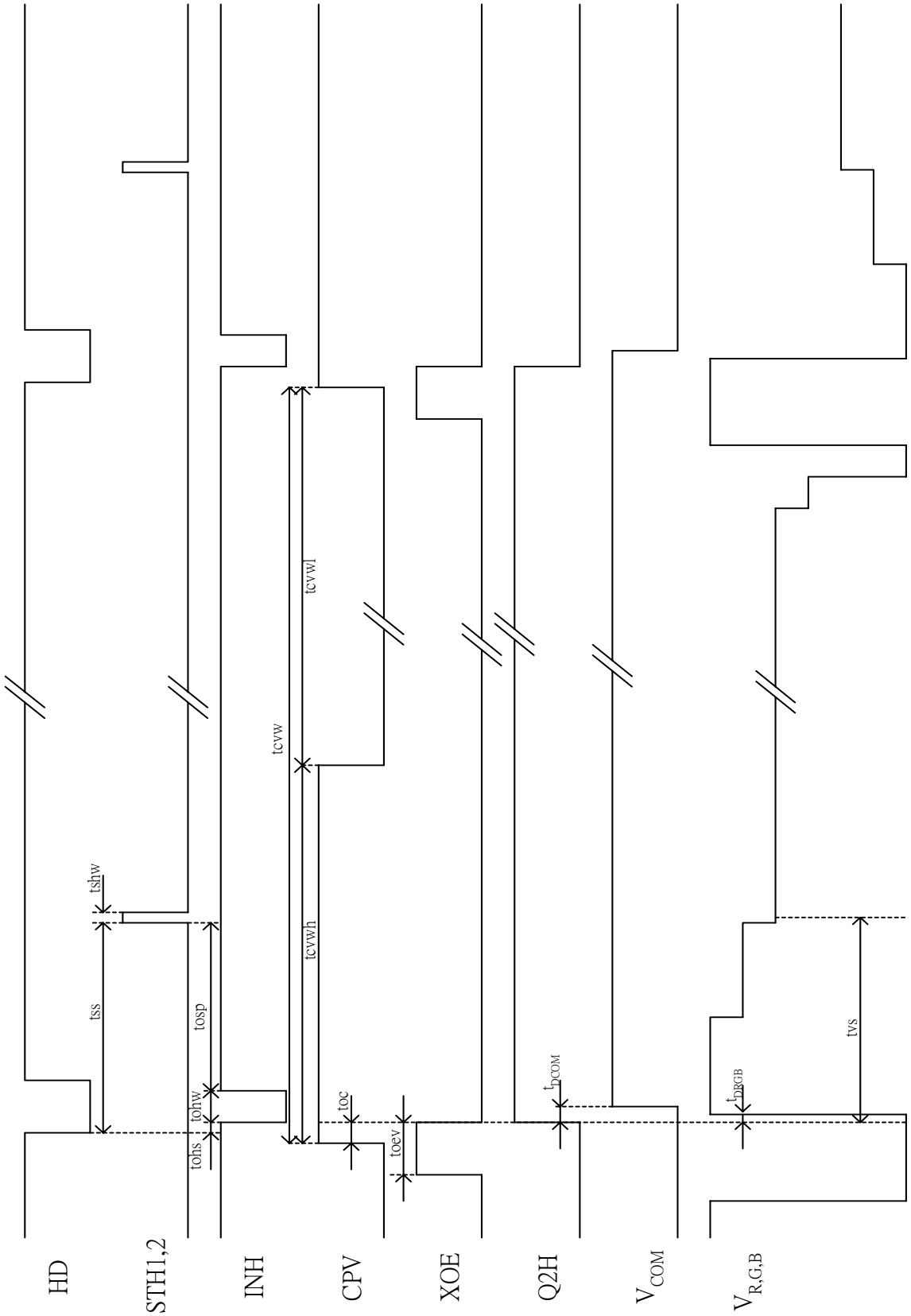


Fig. 8-3 Detail Horizontal Timing

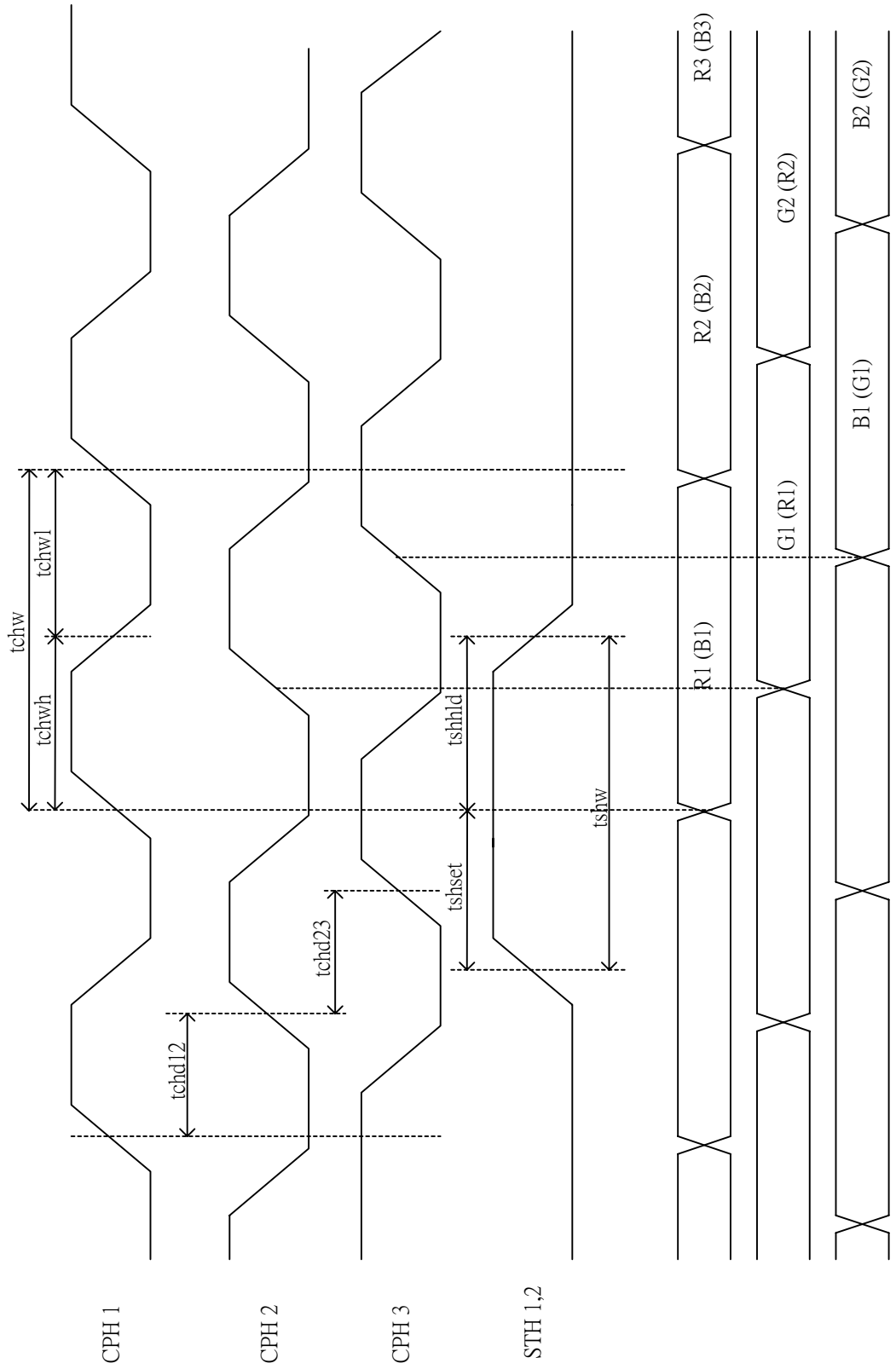


Fig. 8-4 Sampling Clock Timing

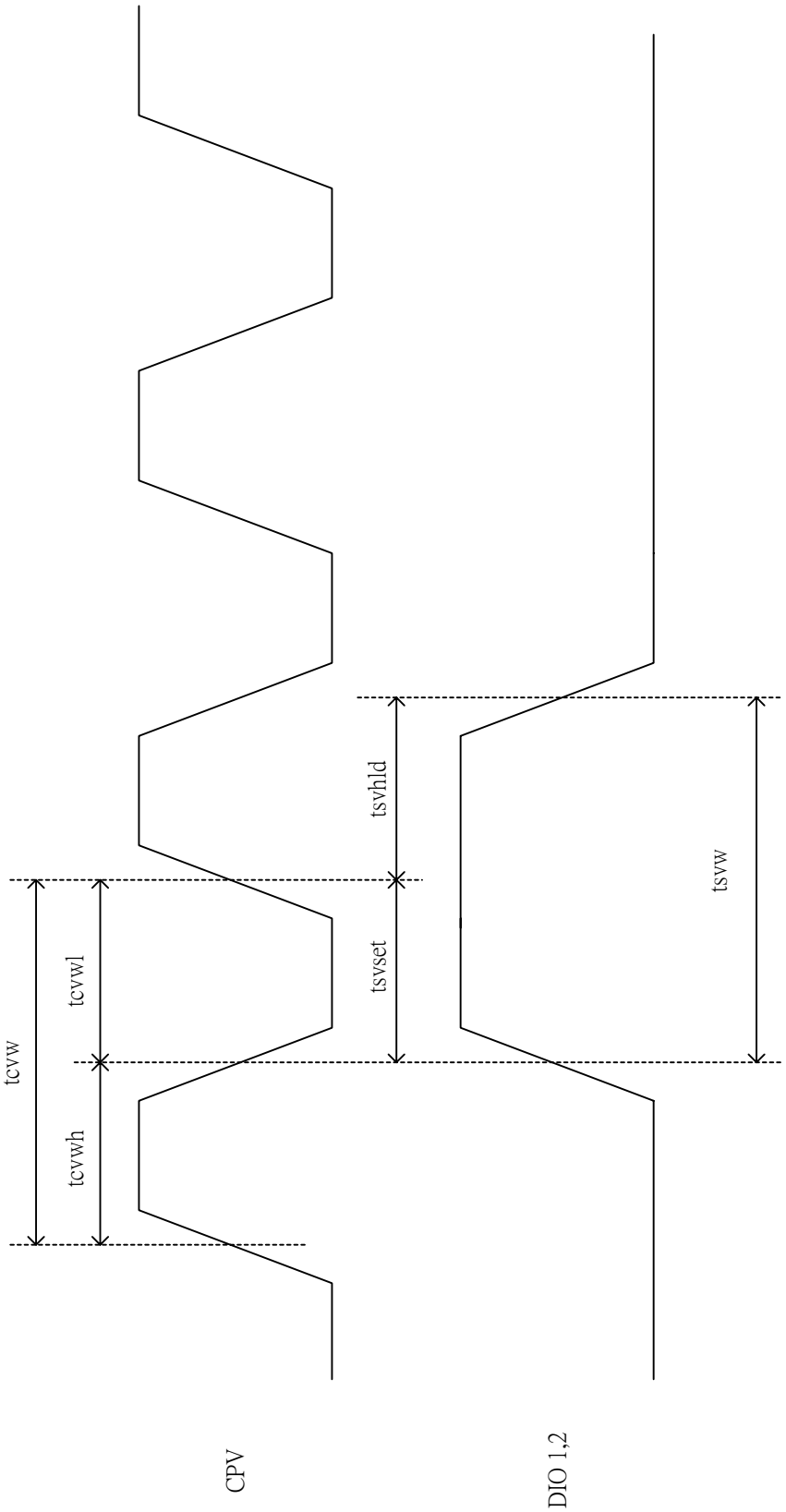


Fig. 8-5 Vertical Shift Clock Timing

Vertical timing (From up to down)

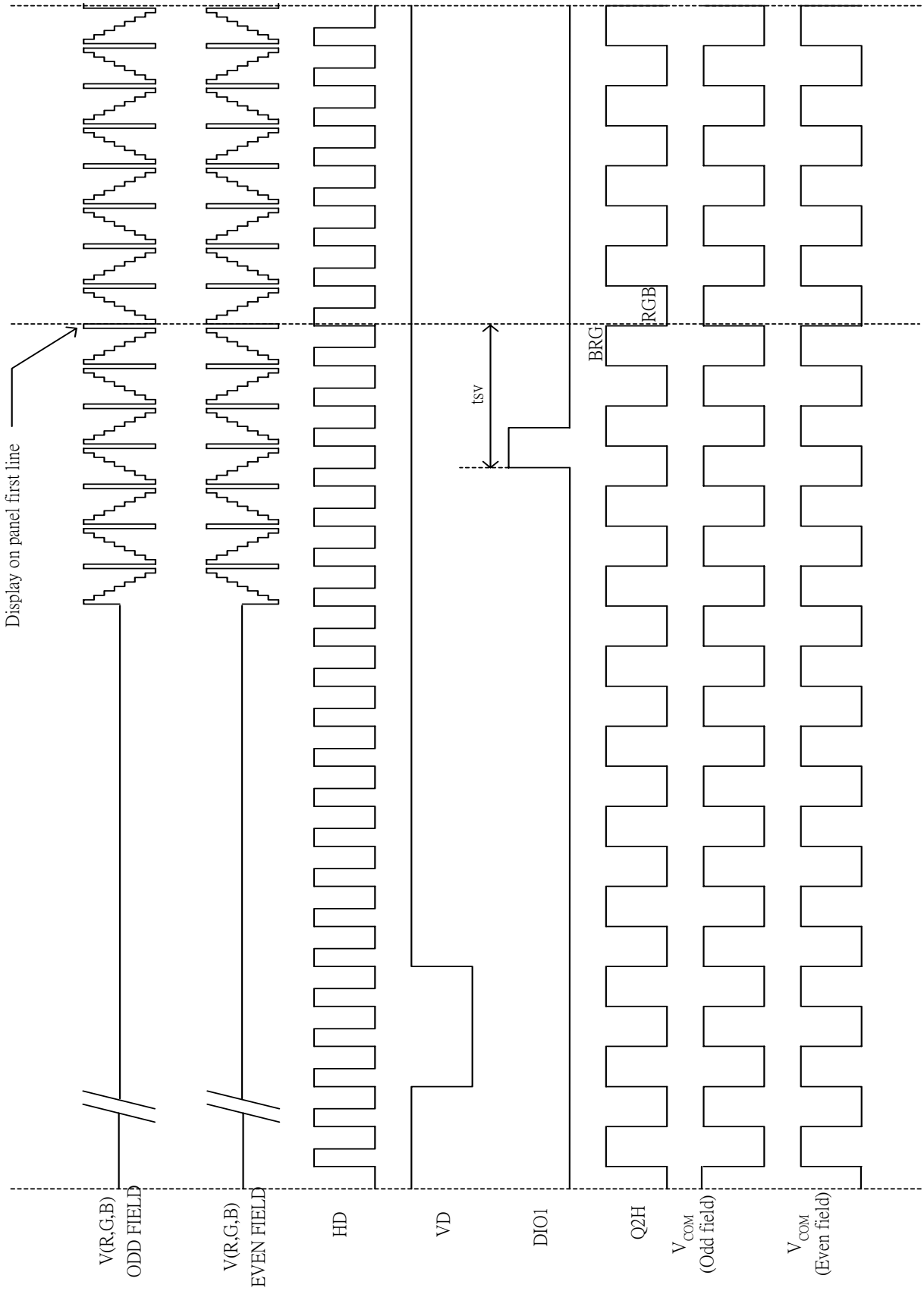


Fig. 8-6(b) Vertical Timing (From Up to Down)

Vertical timing (From down to up)

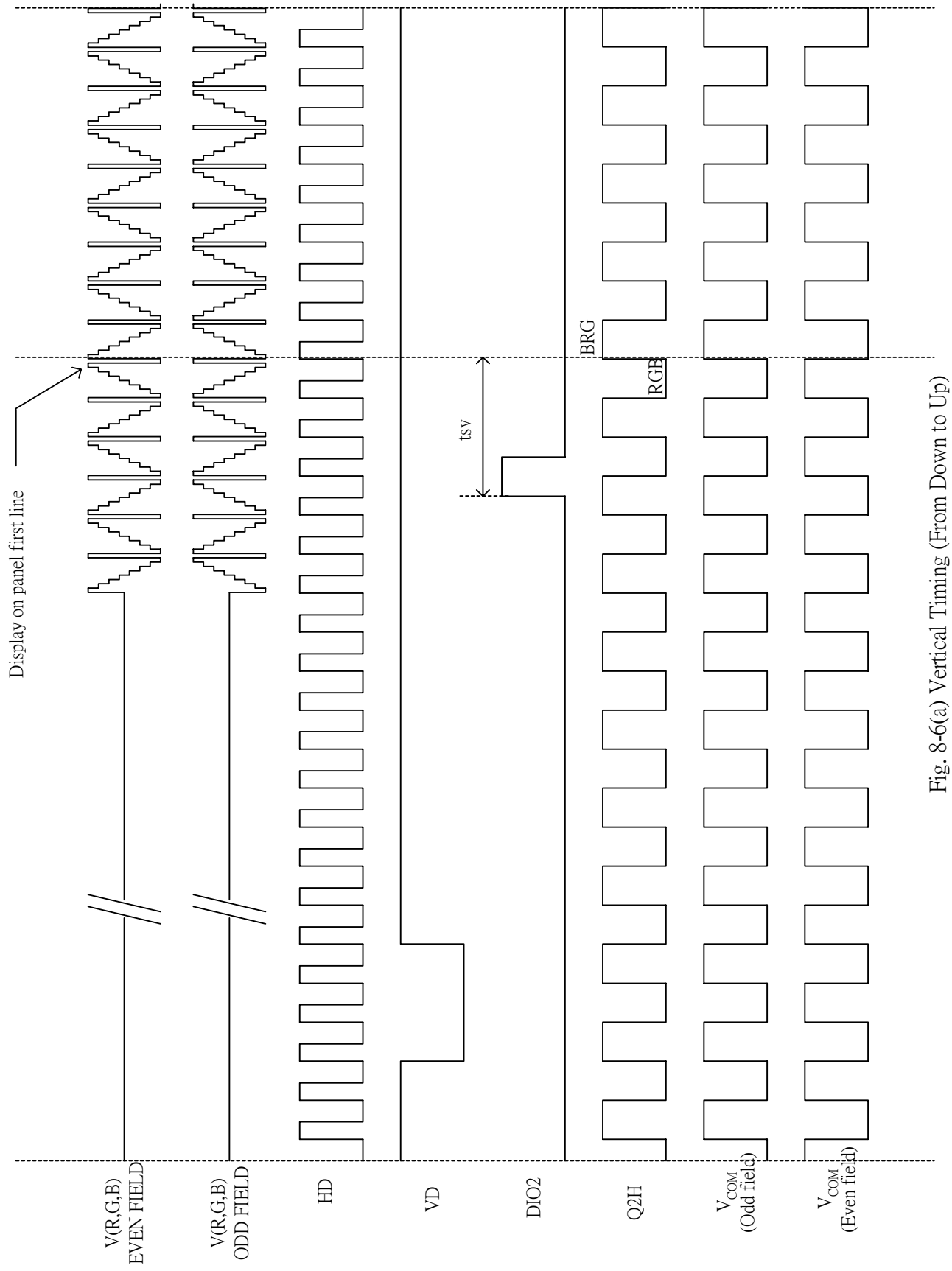
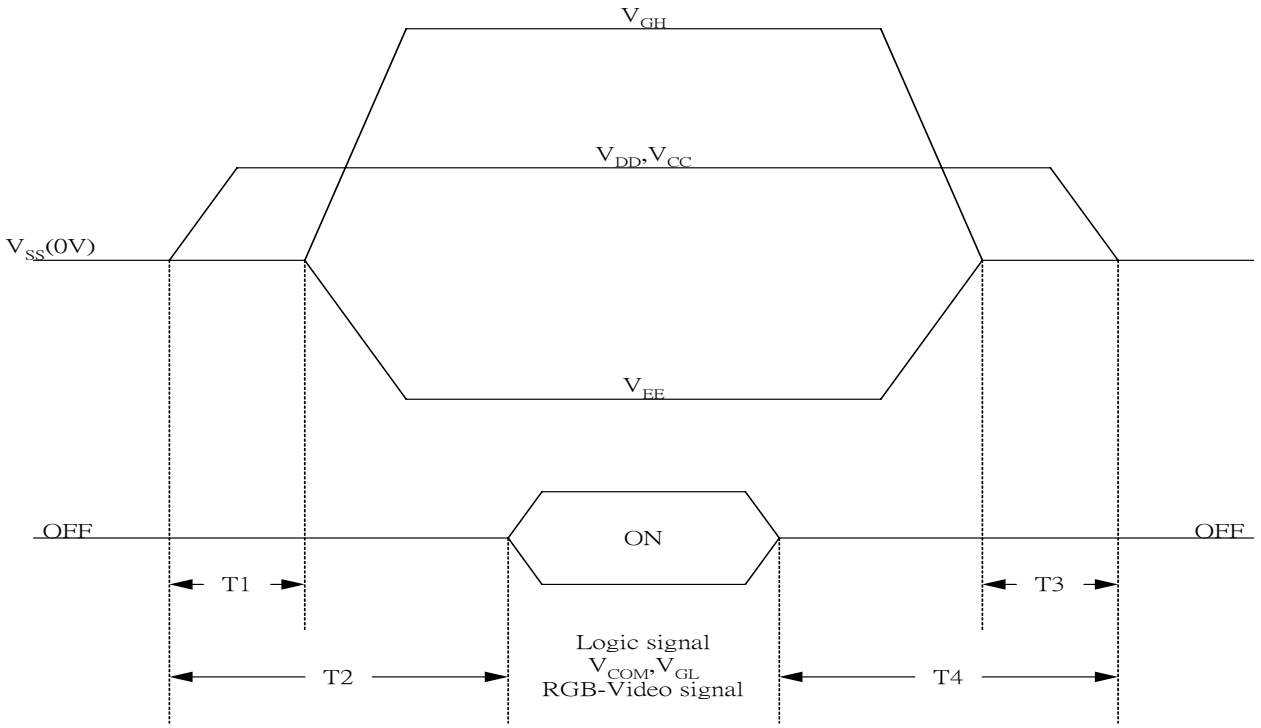


Fig. 8-6(a) Vertical Timing (From Down to Up)

9. Power on Sequence(Voltage source)

The Power on Sequence only effect by V_{CC},V_{SS},V_{DD},V_{EE} and $V_{GH,}$ the others do not care.



1) 10ms≦T1<T2

2) 0ms<T3≦T4≦10ms

10. Optical Characteristics

10-1) Specification

Ta = 25℃

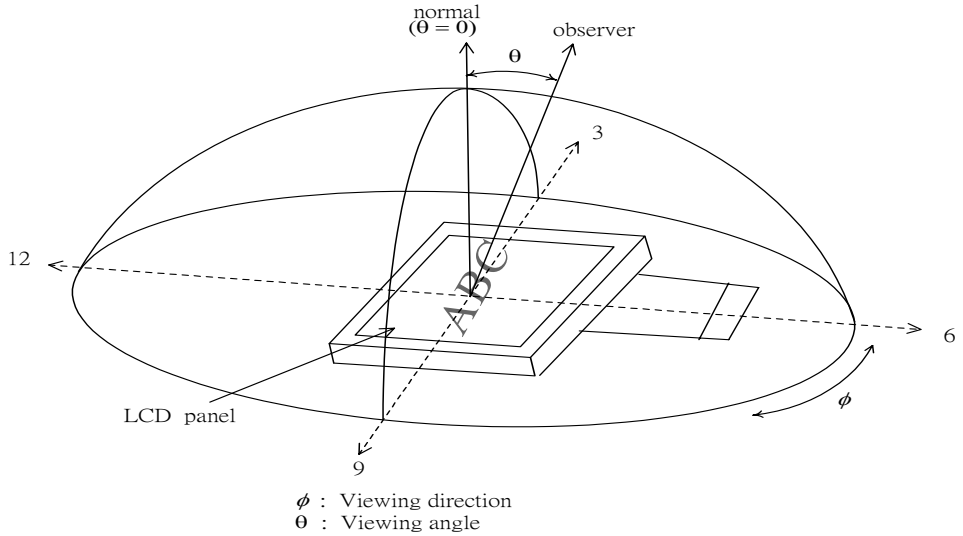
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ	CR≧10	±45	±50		deg	Note 10-3
	Vertical	θ (to 12 o'clock)		10	15		deg	
		θ (to 6 o'clock)		30	35		deg	
Contrast Ratio		CR	At optimized Viewing angle	200	350			Note 10-1
Response time	Rise	Tr	θ =0°		15	30	ms	Note 10-4
	Fall	Tf	φ =0°		25	50	ms	
Uniformity		U		65	70			
Brightness			3mA	200	250		cd/㎡	Note 10-2
			5mA	300	350			
White Chromaticity		X	θ =0°	0.280	0.310	0.340		Note 10-2
		y		0.310	0.340	0.370		
Lamp Life Time	+25℃				30000		hrs	Note 10-5

Note 10-1：CR = $\frac{\text{Luminance when LCD is White}}{\text{Luminance when LCD is Black}}$

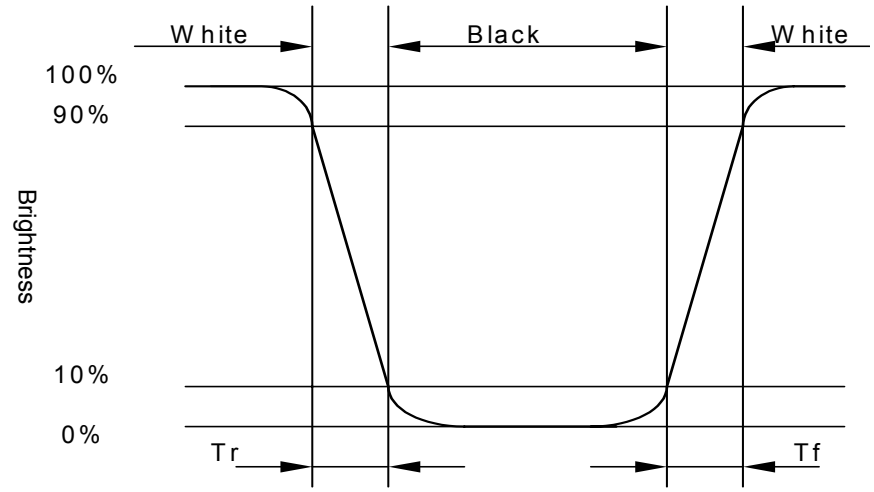
Contrast Ratio is measured in optimum common electrode voltage.
The test configurations of contrast ratio see section 10-2.

Note 10-2：1.Topcon BM-7(fast) luminance meter 1°field of view is used in the testing (after 20~30 minutes operation).
2. Lamp current : 3 mA & 5 mA
3. Inverter model : TDK-347.

Note 10-3：The definition of viewing angle diagrams :

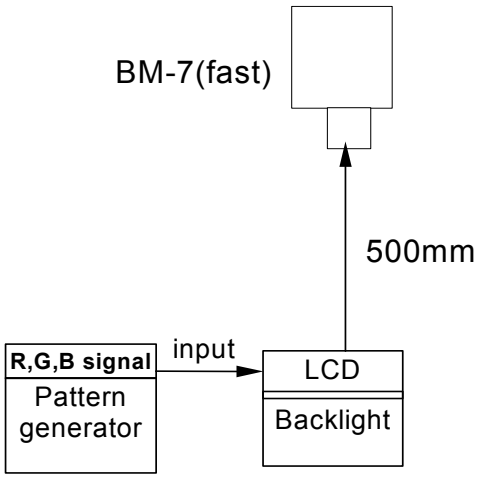


Note 10-4 : The definitions of response time:



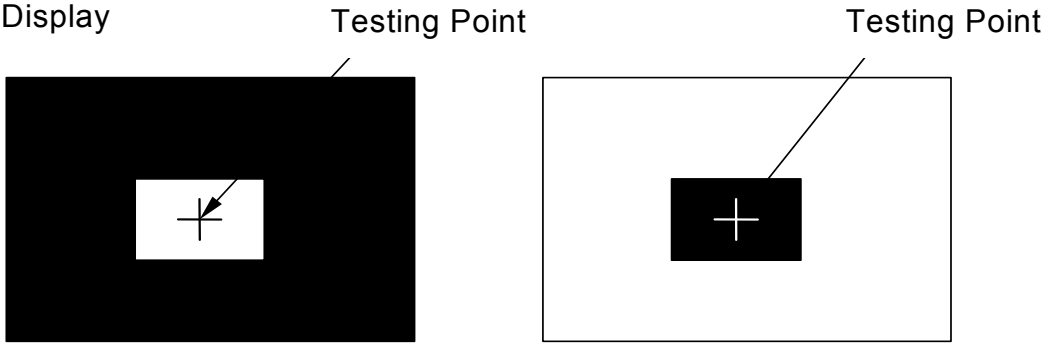
Note 10-5 : Lamp life time 3mA about 30000hrs; 5mA about 20000hrs

10-2) Test Configuration



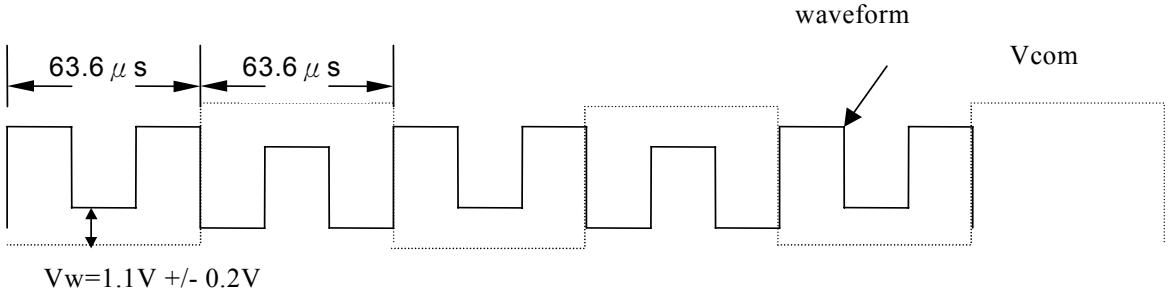
Caution: 1. Environmental illumination ≦ 1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display

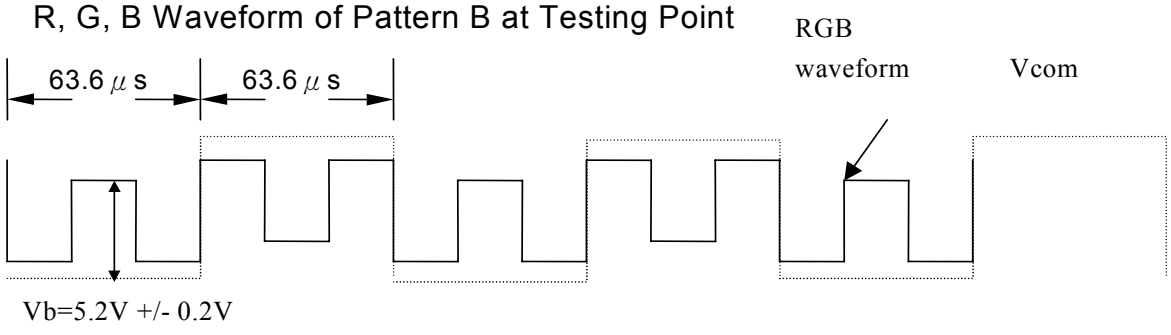


Pattern A Pattern B

- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



11. Handling Cautions

11-1) Mounting of module

a)Please power off the module when you connect the input/output connector.

b) Please connect the ground pattern of the inverter circuit and case surely. If the connection is not perfect, some following problems may happen possibly.

c) The noise from the backlight unit will increase.

1. The output from inverter circuit will be unstable.
2. In some cases a part of module will heat.
3. Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

11-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

11-3) Adjusting module

a) Adjusting volumes on the rear face of the module have been set optimally before shipment.

b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

11-4) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

Please adjust the voltage of common electrode as material of attachment by 1 module.

12. Reliability

No.	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +70 ℃, 240 hrs
2	Low Temperature Storage Test	Ta = -20℃, 240 hrs
3	Low Temperature Operation Test	Ta = 0 ℃, 240 hrs
4	High Temperature & High Humidity Operation Test	Ta = +60℃, 90%RH, 240 hrs
5	Thermal Cycling Test (non-operating)	-25℃ →+70℃, 200 Cycles 30 min 30 min
6	Vibration Test (non-operating)	Frequency：10 ~ 55 H_Z Amplitude：1.0 mm Sweep time: 11 mins Test Period: 6 Cycles for each direction of X, Y, Z
7	Shock Test (non-operating)	100G, 6ms Direction: ±X, ±Y, ±Z Cycle: 3 times
8	Electrostatic Discharge Test (non-operating)	Machine Mode=±200V C=200pF,R=0Ω 1 times discharge for each pad

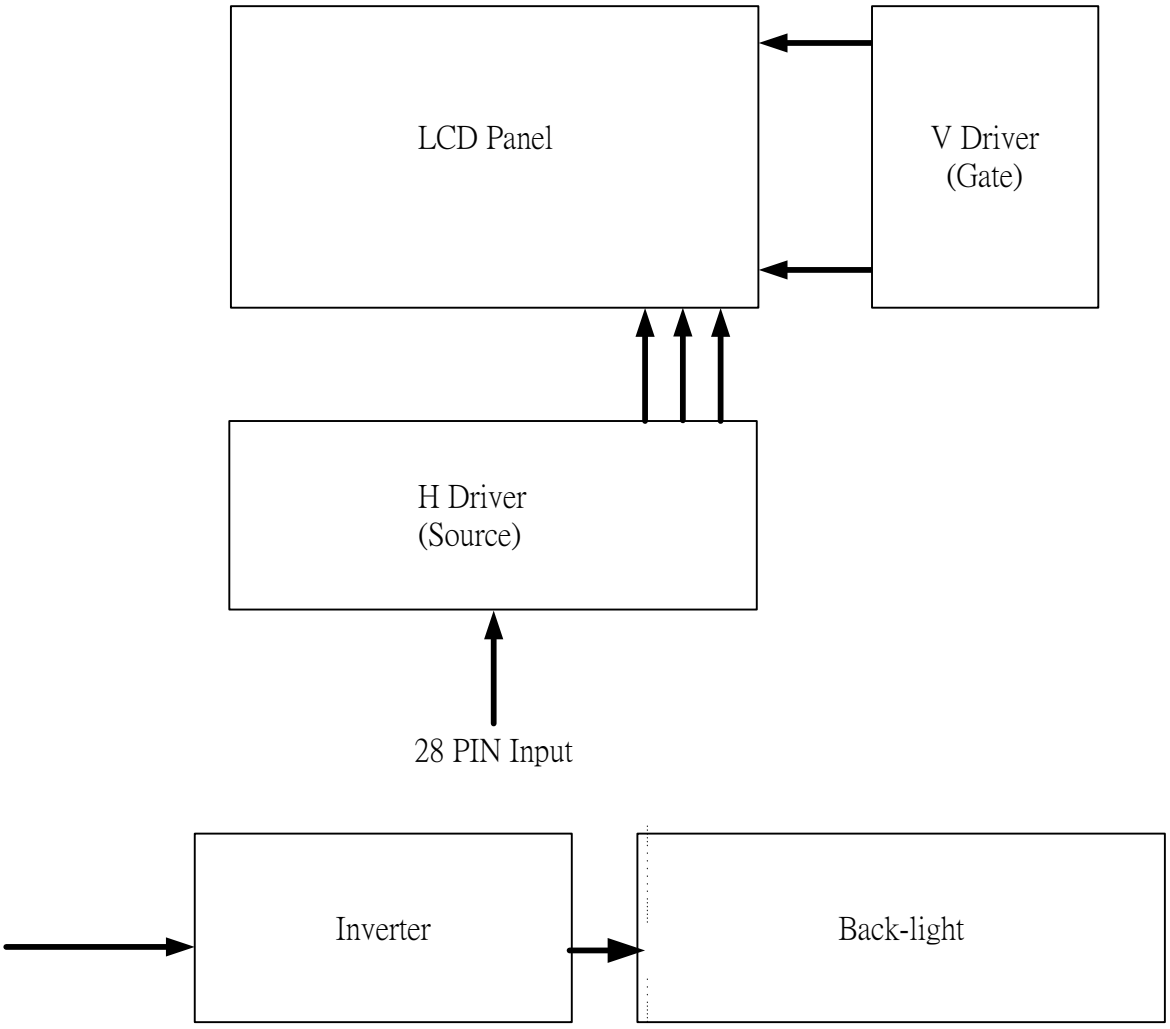
Ta: ambient temperature

Note: The protective film must be removed before temperature test.

[Criteria]

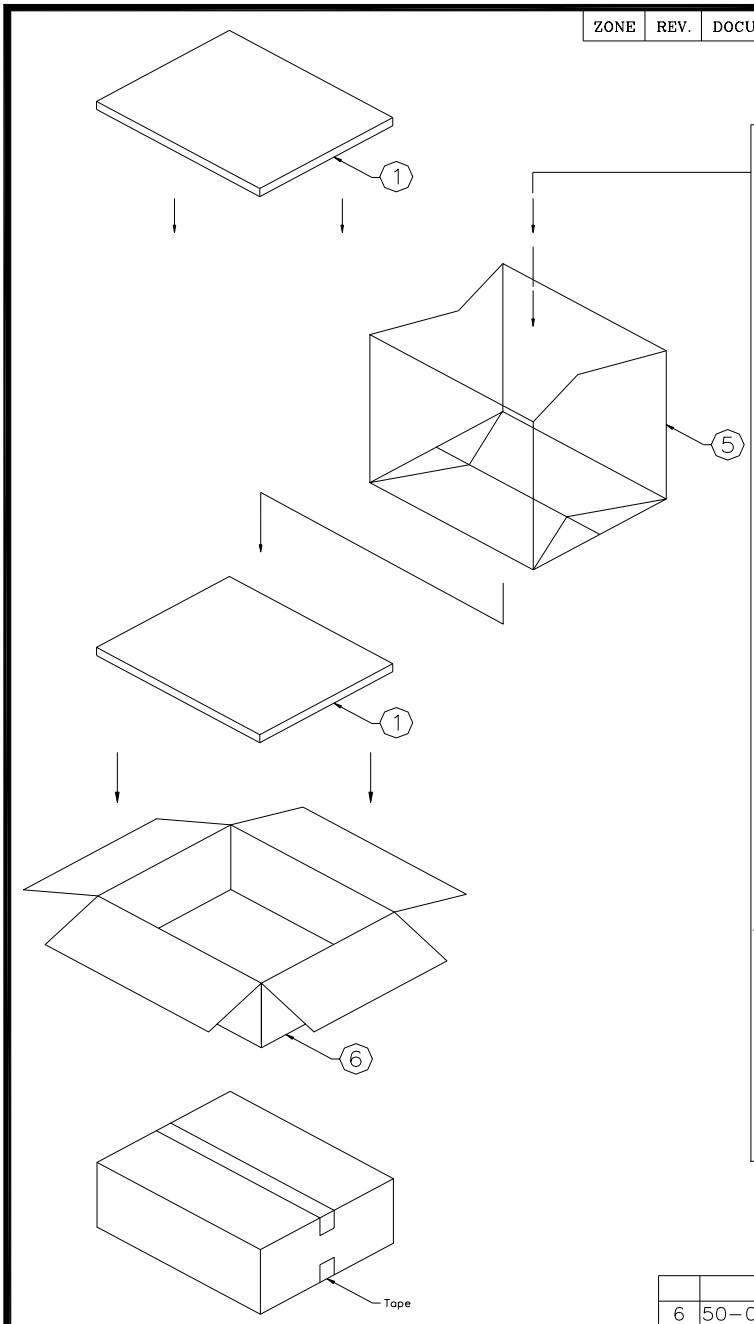
Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

13. Block Diagram



14. Packing

ZONE	REV.	DOCUUMENT NO.	DESCRIPTION	DATE	REV.BY



NOTE:
1. One layer include: 1 piece of cushion sheet, 12pcs panel & 1 piece of tray.
2. Q'TY: 84 pcs panel/carton.
3. Dimension: 455*375*190mm
4. Weight: 7.3 KG

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
6	50-0100091	CARTON INTERNAL	1	
5	50-0500041	摺口袋450*380*700mm	1	抗靜電
4		PA035XS8 Module	84	
3	50-0200004	EPE CUSHION SHEET	7	抗靜電
2	50-0300282	TRAY	8	抗靜電
1	50-0300491	EPE FOAM	2	

MTL.SPEC.	UNSPECIFIED TOL'S	REMARK
	ANGLE	
	ROUGHNESS	

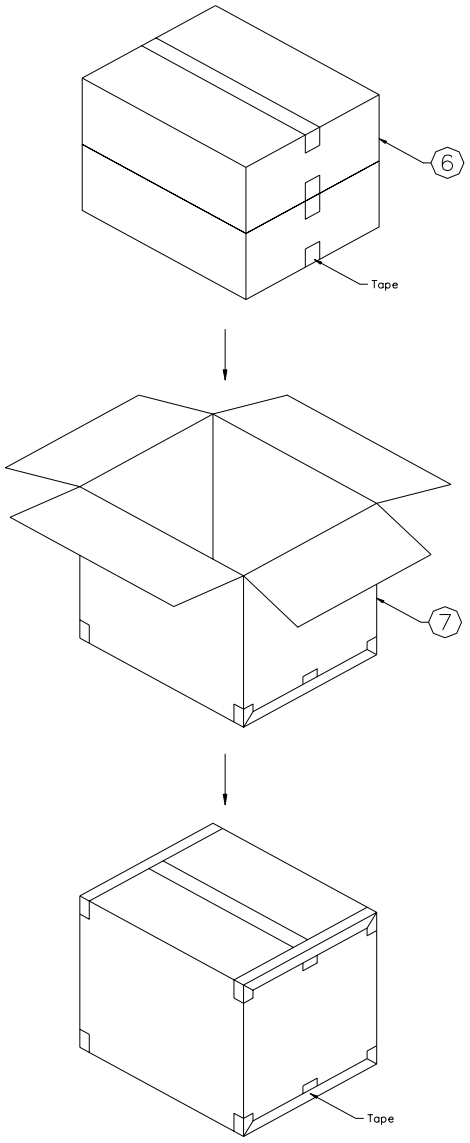
元太科技股份有限公司
Prime View Internation Co.,ltd.

APPROVE		. .	SCALE	UNIT	SHEET 1 OF 2
CHECK		. .			
DESIGN	Jimmy	'04.02.03	MTL.NO.	DWG.NO.	REV. 01

DWG.TITLE: PA035XSE PACKING Draw

A4 SIZE

ZONE	REV.	DOCUUMENT NO.	DESCRIPTION	DATE	REV.BY



NOTE:

1.Q'TY: 168 pcs panel/carton.
2.Dimension: 480*396*405mm
3.Weight: 15.6 KG

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
7	50-0100101	CARTON EXTERNAL	1	

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK	元太科技股份有限公司 Prime View Internation Co.,ltd.

APPROVE		. .	SCALE	UNIT	SHEET 2 OF 2	DWG.TITLE PA035XSE PACKING Draw
CHECK		. .				
DESIGN	Jimmy	'04.02.03	MTL.NO.	DWG.NO.	REV. 01	A4 SIZE

Revision History

Rev.	Issued Date	Revised Contents
0.1	Feb.3,2004	NEW
1.0	Mar.2,2004	Updata Page:24 12. Reliability test Vibration Test& ShockTest ok
1.1	Oct.6,2004	Updata Page9:Note 8-5 B/L Lamp voltage kick-off time
1.2	Oc.21,2004	Modify Page 10: 8-5) Timing Characteristics Of Input Signals Page 13: Fig.8-2 Horizontal Start Pixel
1.3	Jan.20,2005	Updata: Page 20: Lamp current about 5mA brightness & lamp life time.