Version :1.0

TECHNICAL SPECIFICATION

MODEL NO. : PW070XU3

☐Customer's Confirmation

Customer

Date

By

☐PVI's Confirmation

Confirmed By

Date : Mar.08,2005

This technical specification is subject to change without notice.
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TECHNICAL SPECIFICATION

CONTENTS

1. Application

This technical specification applies to 7.0” color TFT-LCD module, PW070XU3.
The applications of the panel are car TV, portable DVD, GPS, multimedia applications and others AV system.

2. Features

. Amorphous silicon TFT-LCD with B/L unit

. Pixel in stripe configuration

. Slim and compact

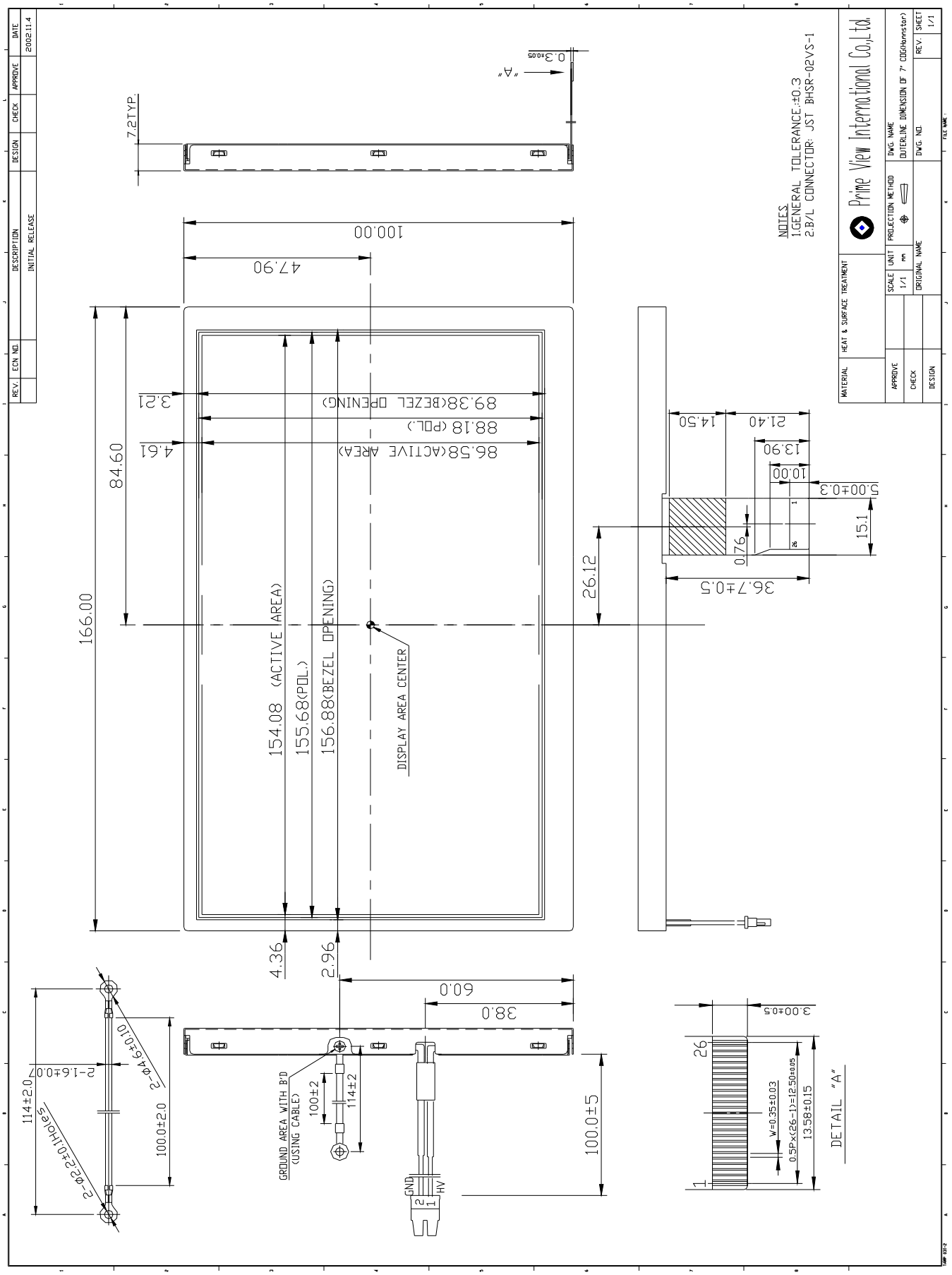
. Image Reversion：Up/Down and Left/Right

. Support multi display mode
(If you use this mode, you must use PVI-1004D’s timing controller (made by PVI))

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	7.0 (16:9 diagonal)	Inch
Display Format	1440 (H) ×234(V)	dot
Active Area	154.08 (H)×86.58 (V)	mm
Dot Pitch	0.107(H)×0.370 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	166.0(W)x100.0(H)x7.2(D)(Typ.)	mm
Surface Treatment	Anti-Glare and Hard Coating	
Weight	164±10	g

4. Mechanical Drawing of TFT-LCD Module



5.Input / Output Terminals

LCD Module Connector
FPC Down Connect , 26 Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	GND	-	Ground for logic circuit	
2	V_{CC1}	I	Supply voltage of logic control circuit for scan driver	
3	V_{GL}		Negative power for scan driver	
4	V_{GH}	I	Positive power for scan driver	
5	STVD	I/O	Vertical start pulse	Note 5-1
6	STVU	I/O	Vertical start pulse	Note 5-1
7	CKV	I	Shift clock for scan driver	
8	U/D	I	Up / Down scan control input	Note 5-1
9	OEV	I	Output enable control for scan driver	
10	V_{COM}	I	Common electrode driving signal	
11	V_{COM}	I	Common electrode driving signal	
12	L/R	I	Left / Right control	Note 5-2
13	MOD	I	Sequential sampling and simultaneous sampling setting	Note 5-3
14	OEH	I	Output enable control for data driver	
15	STHL	I/O	Start pulse for horizontal scan line	Note 5-2
16	STHR	I/O	Start pulse for horizontal scan line	Note 5-2
17	CPH3	I	Sampling and shifting clock for data driver	
18	CPH2	I	Sampling and shifting clock for data driver	
19	CPH1	I	Sampling and shifting clock for data driver	
20	V_{CC2}	I	Supply voltage of logic control circuit for data driver	
21	GND	-	Ground for logic circuit	
22	VR	I	Alternated video signal (Red)	
23	VG	I	Alternated video signal (Green)	
24	VB	I	Alternated video signal (Blue)	
25	AV_{DD}	I	Supply voltage for analog circuit	
26	AV_{SS}	I	Ground for analog circuit	

Note 5-1

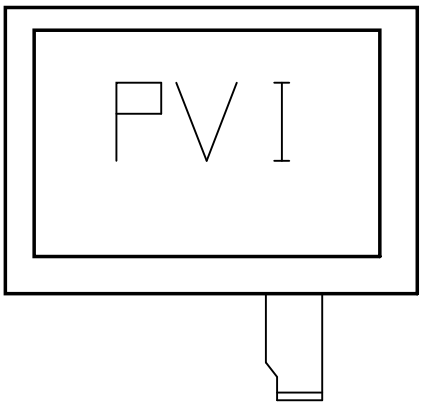
U/D	STVD	STVU	scanning direction
Vcc	Input	output	down to up
GND	Output	input	up to down

Note 5-2

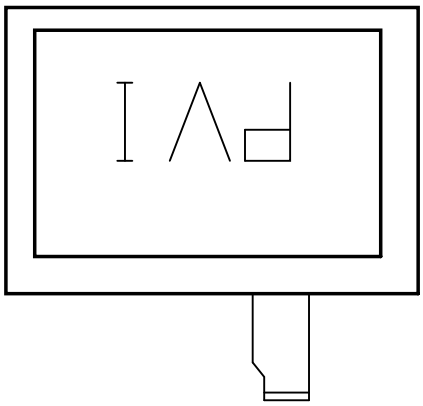
R/L	STHL	STHR	scanning direction
Vcc	output	input	left to right
GND	input	output	right to left

The definitions of Note 5-1

U/D(PIN 8)=Low R/L(PIN 12)=High



U/D(PIN 8)=High R/L(PIN 12)=Low



Note 5-3 : MOD=H: Simultaneous sampling
MOD=L: Sequential sampling
Please set CPH2 and CPH3 to GND when MOD=H

Note 5-4 : V_{CC1} TYP.＝+3.3V

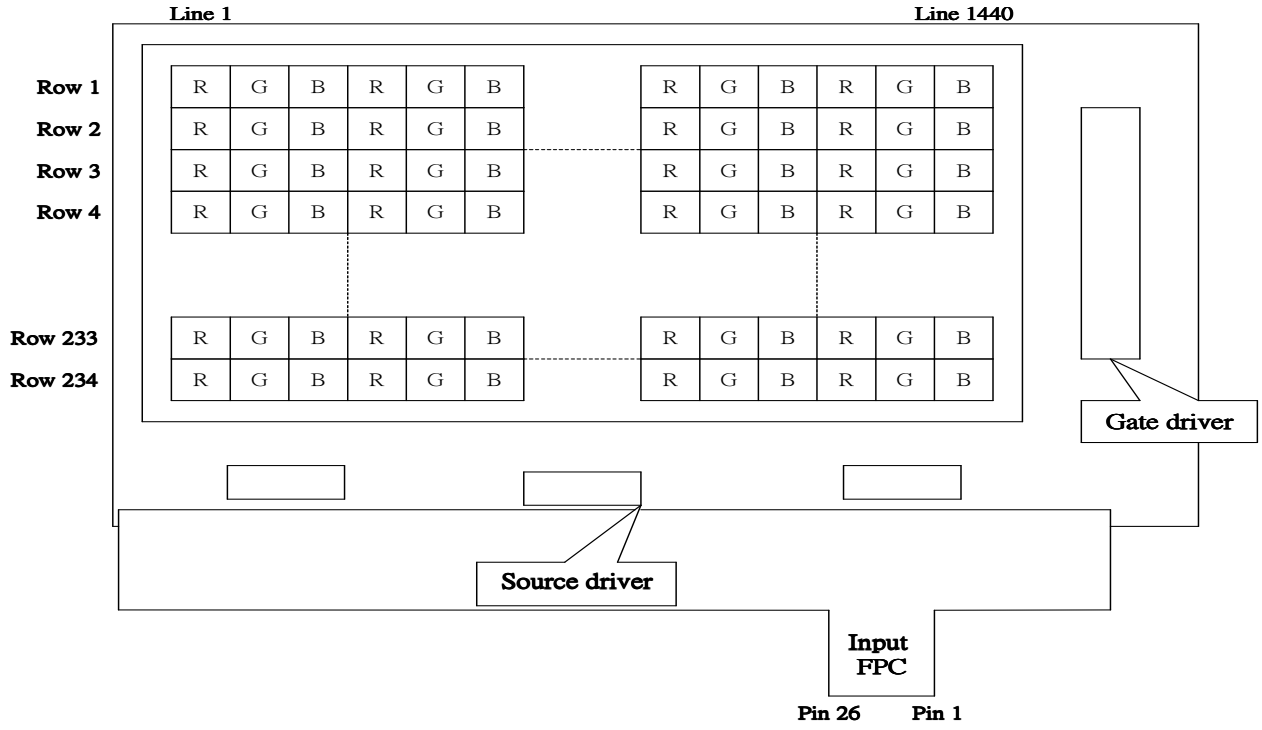
Note 5-5 : V_{GL} TYP.＝-12V

Note 5-6 : V_{GH} TYP.＝+17V

Note 5-7 : V_{CC2} TYP.＝+3.3V

Note 5-8 : AV_{DD} TYP.＝+5V

6. Pixel Arrangement and input connector pin No.



7.Absolute Maximum Ratings

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage For Source Driver		AV_{DD}	-0.3	+7.0	V	
		V_{CC2}	-0.3	+6.0	V	
Supply Voltage For Gate Driver		V_{CC1}	-0.3	+6.0	V	
	H Level	V_{GH}	-0.3	+30	V	
	L Level	V_{GL}	-20	+0.3	V	
		V_{GH} -V_{GL}	-0.3	+40	V	
Analog Input Signal Voltage		V_R,V_G,V_B	-0.3	AV_{DD} +0.3	V	Note 7-1
Storage Temperature			-20	+70	℃	
Operation Temperature			0	+60	℃	Note 7-2

Notes 7-1 : Analog Input Voltage means V_R,V_G,V_B.

Notes 7-2: Optical characteristics shown in Table 10-1 are measured under Ta=+25℃.

8. Electrical Characteristics

8-1) Recommended Driving condition for TFT-LCD panel

Parameter		Symbol	MIN.	Typ.	MAX.	Unit	Remark
Supply Voltage For Source Driver	Analog	AV_{DD}	+4.5	+5.0	+5.5	V	
	Logic	V_{CC2}	+3.0	+3.3	+3.6	V	
Supply Voltage For Gate Driver	H level	V_{GH}	+15	+17	+19	V	
	L level	$V_{GL\ DC}$	-13.0	-12	-10.5	V	DC component
		$V_{GL\ AC}$		+5.0			AC component
	Logic	V_{CC1}	+3.0	+3.3	+3.6	V	
Analog Input Signal Voltage	V_{IAC}	V_{iAC}	-	+4.0	+4.2	V	AC component
	V_{IDC}	V_{iDC}	-	2.5	-	V	DC component
Digital input voltage	H level	V_{IH}	0.7 V_{CC}	-	V_{CC}	V	
	L level	V_{IL}	0	-	0.3 V_{CC}	V	
Digital output voltage	H level	V_{OH}	0.7 V_{CC}	-	V_{CC}	V	
	L level	V_{OL}	0	-	0.3 V_{CC}	V	
V_{COM}		$V_{COM\ AC}$	-	+5.0	-	V_{p-p}	AC component of V_{COM}
		$V_{COM\ DC}$	-	1.6	-	V	DC component of V_{COM} Note 8-1

Note 8-1 : PVI strongly suggests that the $V_{COM\ DC}$ level shall be adjustable , and the adjustable level range is 1.6V±1V , every module's $V_{COM\ DC}$ level shall be carefully adjusted to show a best image performance.

8-2)Recommended driving condition for back light

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	474	527	580	Vrms	I_L=6mA
Lamp current	I_L	3	6	8	MA	Note 8-2
Lamp frequency	P_L	40	55	80	KHz	Note 8-3
Kick-off voltage(25℃) (Reference Value)	Vs			630	Vrms	Note 8-4
Kick-off voltage(0℃) (Reference Value)	Vs			890	Vrms	Note 8-4

Note 8-2 : In order to satisfy the quality of B/L , no matter use what kind of inverter , the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 8-3 : The waveform of lamp driving voltage should be as closed to a perfect sine wave as possible.

Note 8-4 : The Kick-off times≧1sec.

Back Light driving

Back Light Connector : JST BHSR-02VS-1, Pin No. : 2 , Pitch : 3.5 mm

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
2	VL2	Input terminal (Low voltage side)	Note 8-5

Note 8-5 : Low voltage side of back light inverter connects with Ground of inverter circuits.

8-3) Power Consumption

Ta= 25 ℃

Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
Supply current for Gate Driver (Hi level)	I_{GH}	V_{GH} = +17V	0.6	0.9	mA	
Supply current for Gate Driver (Low level)	I_{GL}	V_{GL} = -12V	1.5	1.9	mA	
Supply current for Source Driver(Analog)	I_{DD}	AV_{DD} =+5V	10.5	15	mA	
Supply current for Source Driver(Digital)	I_{CC2}	V_{CC2} = +3.3V	1.1	1.35	mA	
Supply current for Gate Driver (Digital)	I_{CC1}	V_{CC1} = +3.3V	0.2	0.5	mA	
LCD Panel Power Consumption			85	120	mW	Note 8-6
Back Light Lamp Power Consumption			3.3		W	Note 8-7

Note 8-6 : The power consumption for back light is not included.

Note 8-7 : Back light lamp power consumption is calculated by $I_L \times V_L$.

8-3) Timing Characteristics Of Input Signals

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
Rising time	t_r	-	-	10	ns	
Falling time	t_f	-	-	10	ns	
High and low level pulse width	t_{CPH}	9.2	9.6	10.0	MHz	CPH1~CPH3
CPH pulse duty	t_{CWH}	30	50	70	%	CPH1~CPH3
STH setup time	t_{SUH}	20	-	-	ns	STHR,STHL
STH hold time	t_{HDH}	20	-	-	ns	STHR,STHL
STH pulse width	t_{STH}	-	1	-	t_{CPH}	STHR,STHL
STH period	t_H	61.5	63.5	65.5	μs	STHR,STHL
OEH pulse width	t_{OEH}	-	1.40	-	μs	OEH
Sample and hold disable time	t_{DIS1}	-	7.43	-	μs	
OEV pulse width	t_{OEV}	-	18	-	μs	OEV
CKV pulse width	t_{CKV}	-	31.75	-	μs	CKV
Clean enable time	t_{DIS2}	-	9.0	-	μs	
Horizontal display start	t_{SH}	-	0	-	t_{CPH}/3	
Horizontal display timing range	t_{DH}	-	480	-	t_{CPH}	
STV setup time	t_{SUV}	400	-	-	Ns	STVR,STVL
STV hold time	t_{HDV}	400	-	-	Ns	STVR,STVL
STV pulse width	t_{STV}	-	-	1	t_H	STVR,STVL
Horizontal lines per field	t_V	256	262	268	t_H	
Vertical display start	t_{SV}		3	-	t_H	
Vertical display timing range	t_{DV}		234	-	t_H	
VCOM rising time	t_{rCOM}		-	5	Ms	
VCOM falling time	t_{fCOM}		-	5	Ms	
VCOM delay time	t_{DCOM}		-	3	Ms	
RGB delay time	t_{DRGB}		-	1	Ms	

8-4) Signal Timing Waveforms

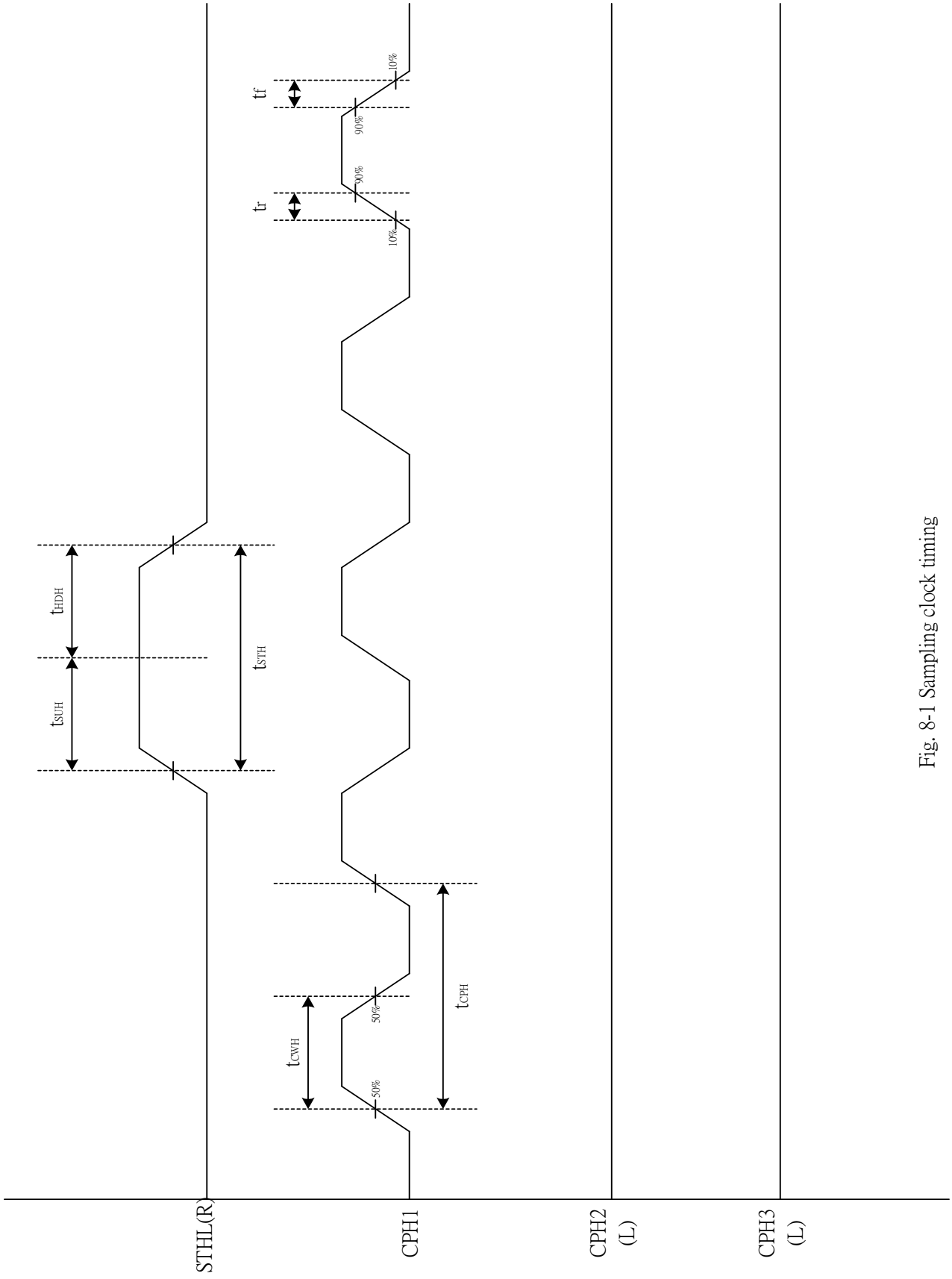


Fig. 8-1 Sampling clock timing

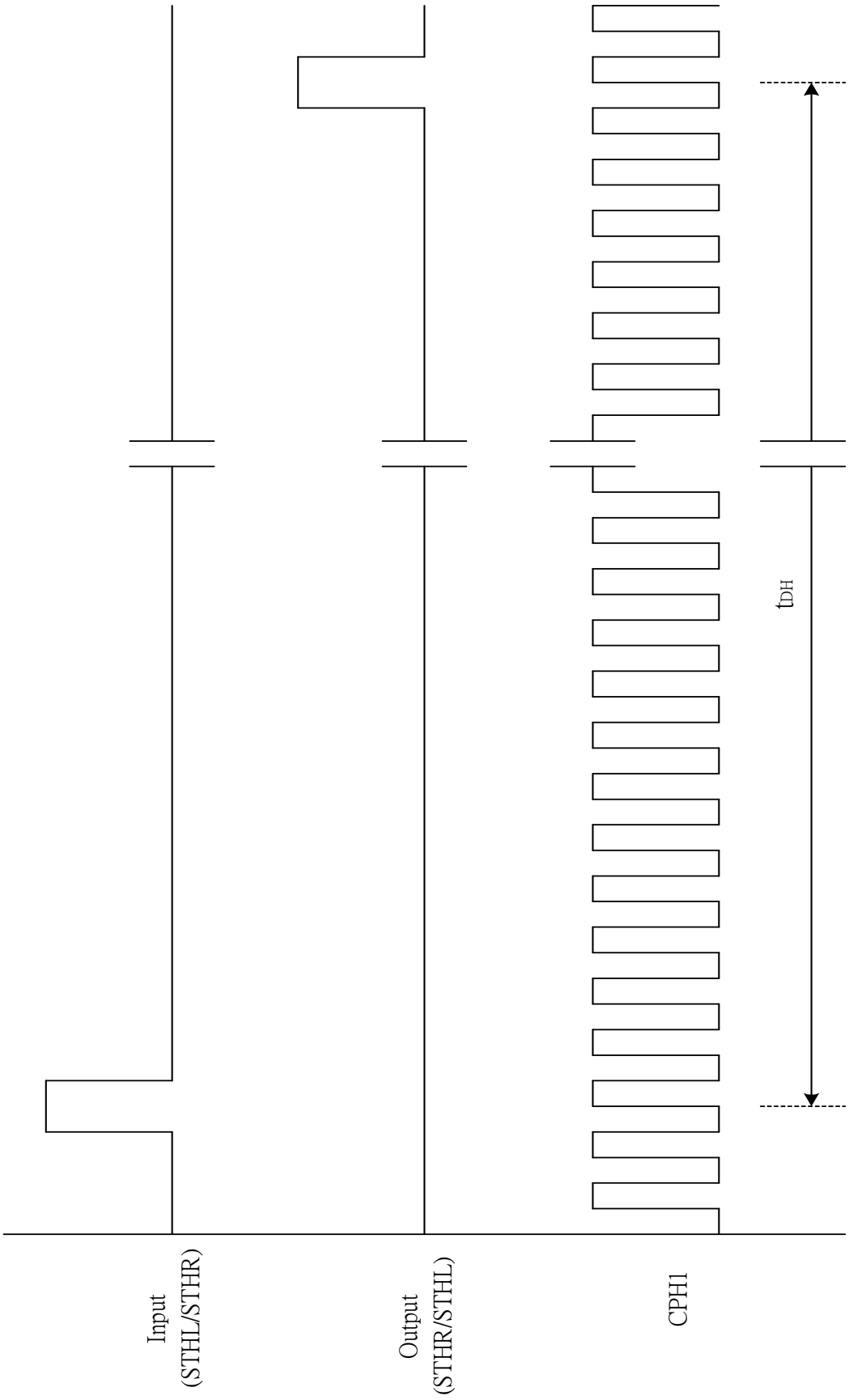


Fig. 8-2 Horizontal display timing range

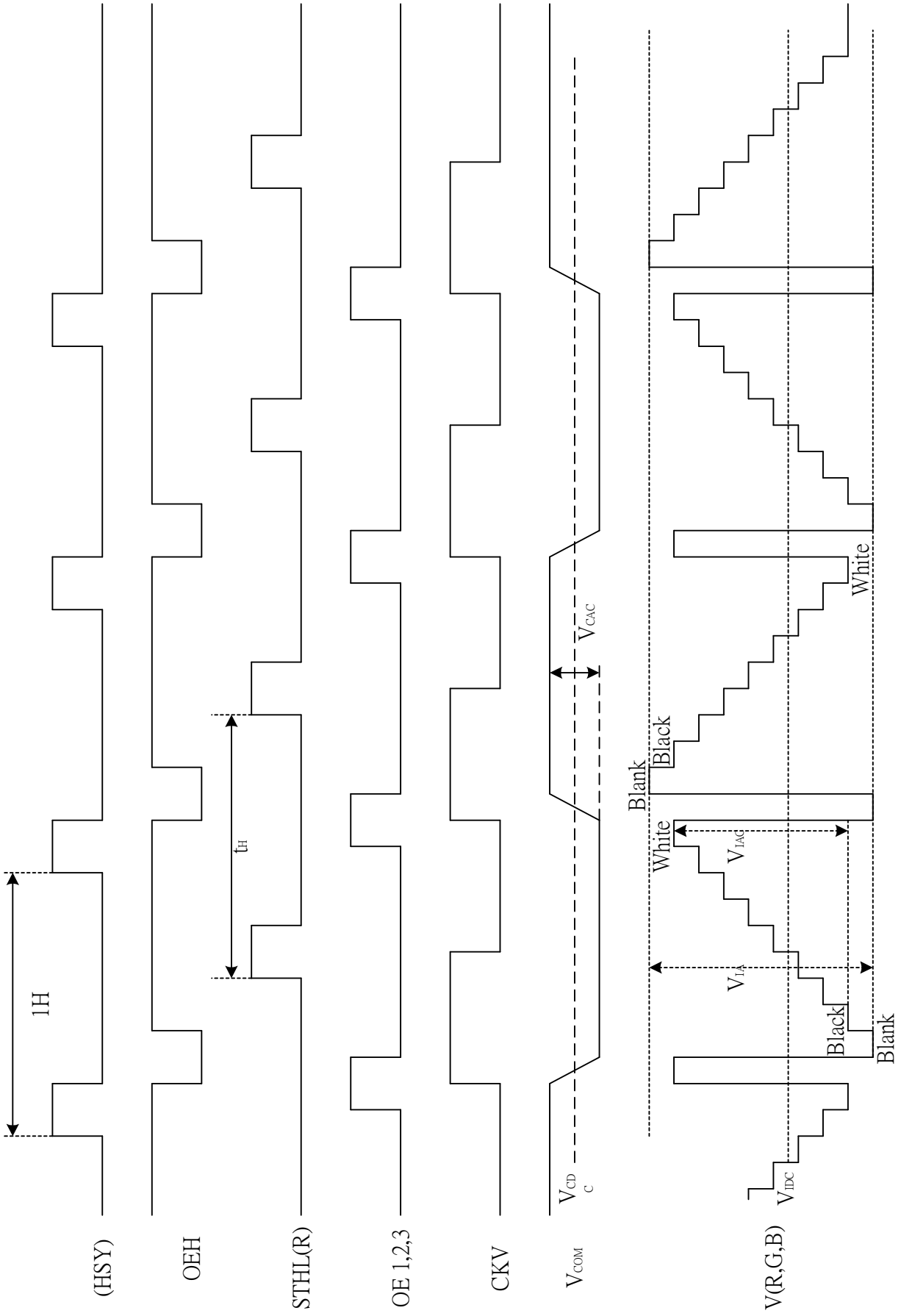
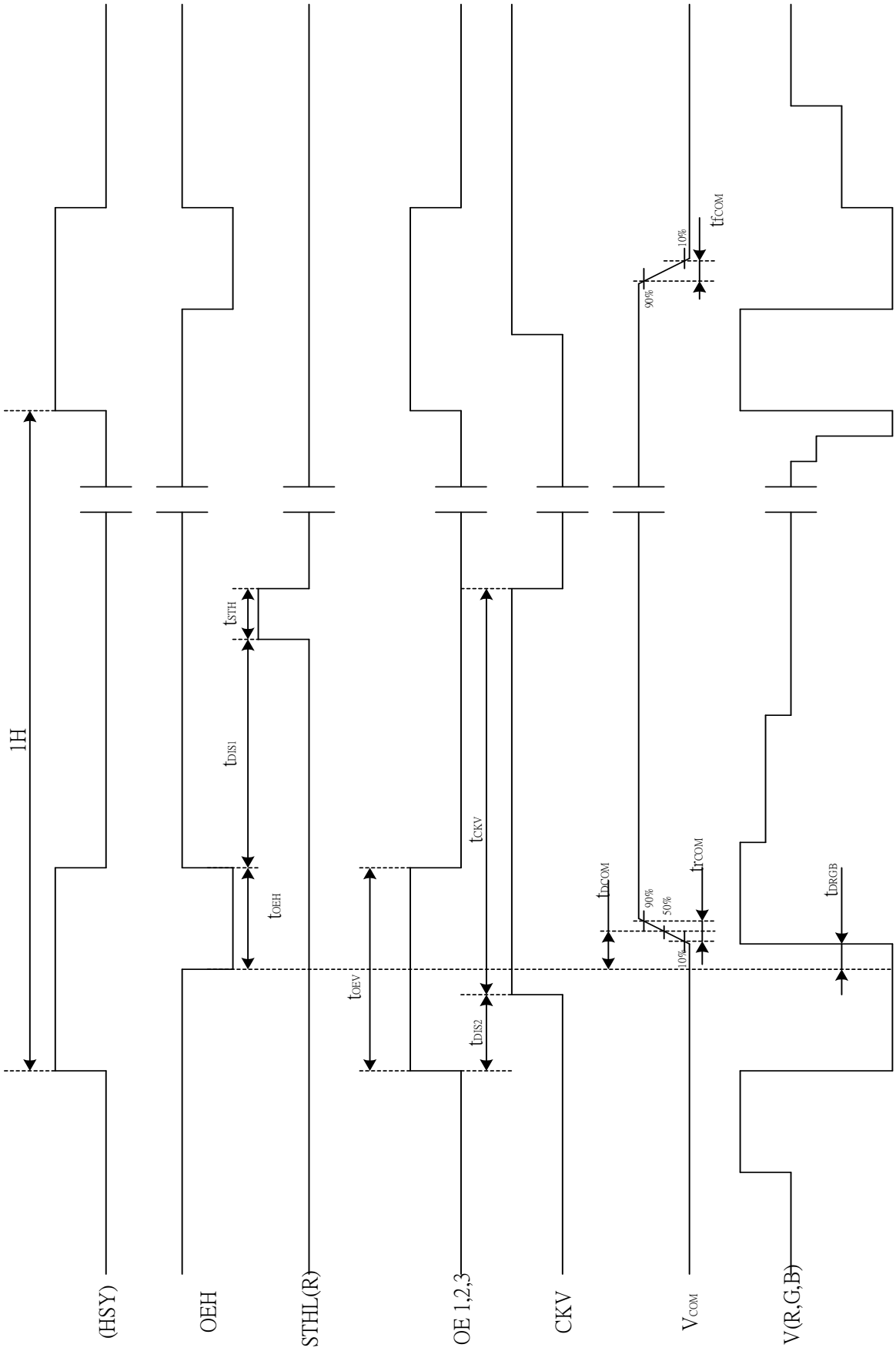


Fig. 8-3 (a) Horizontal timing



Note : The falling edge of OEV should be synchronized with the falling edge of OEH

Fig. 8-3 (b) Detail horizontal timing

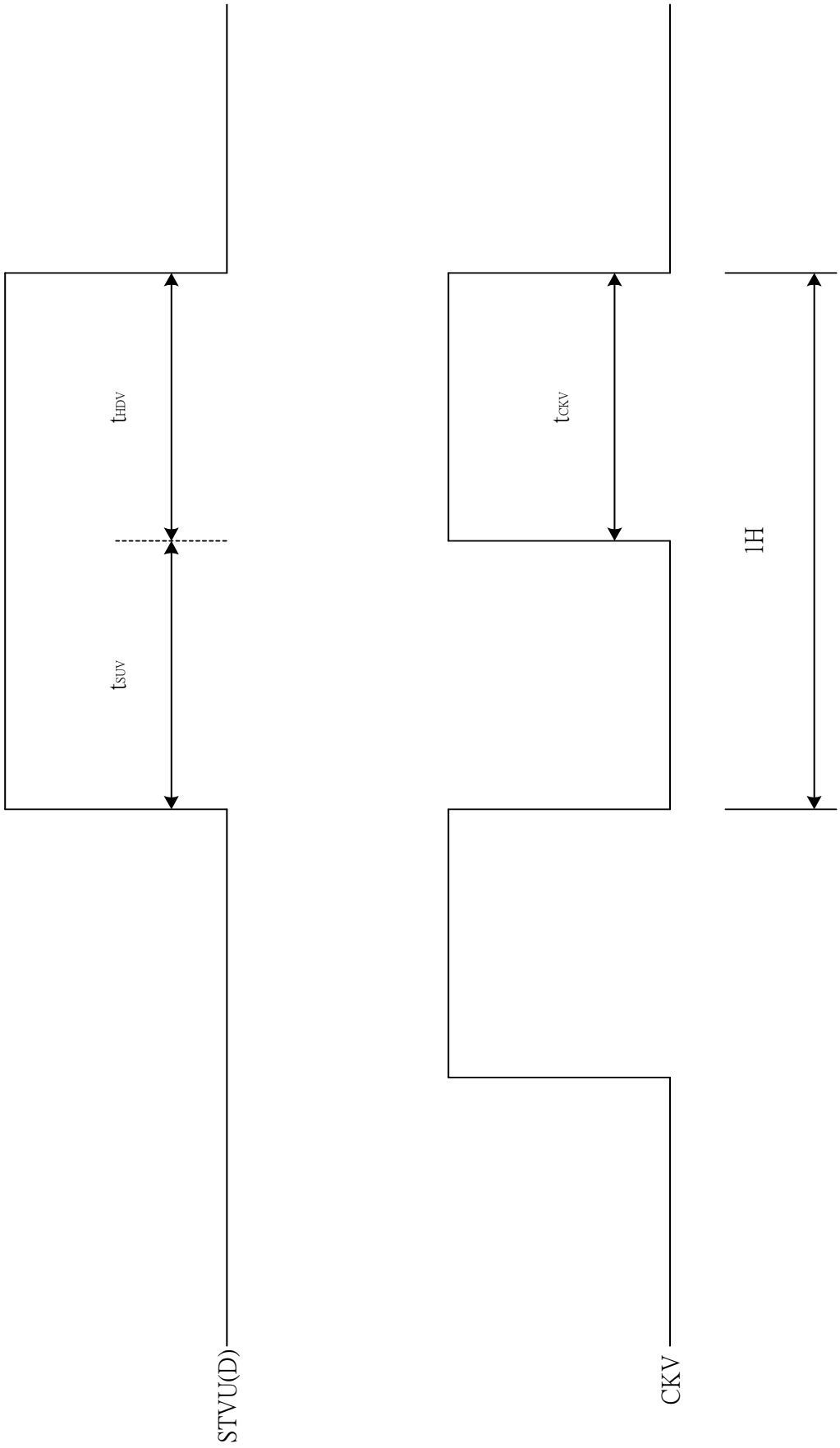


Fig. 8-4 Vertical shift clock timing

Vertical timing (From up to down)

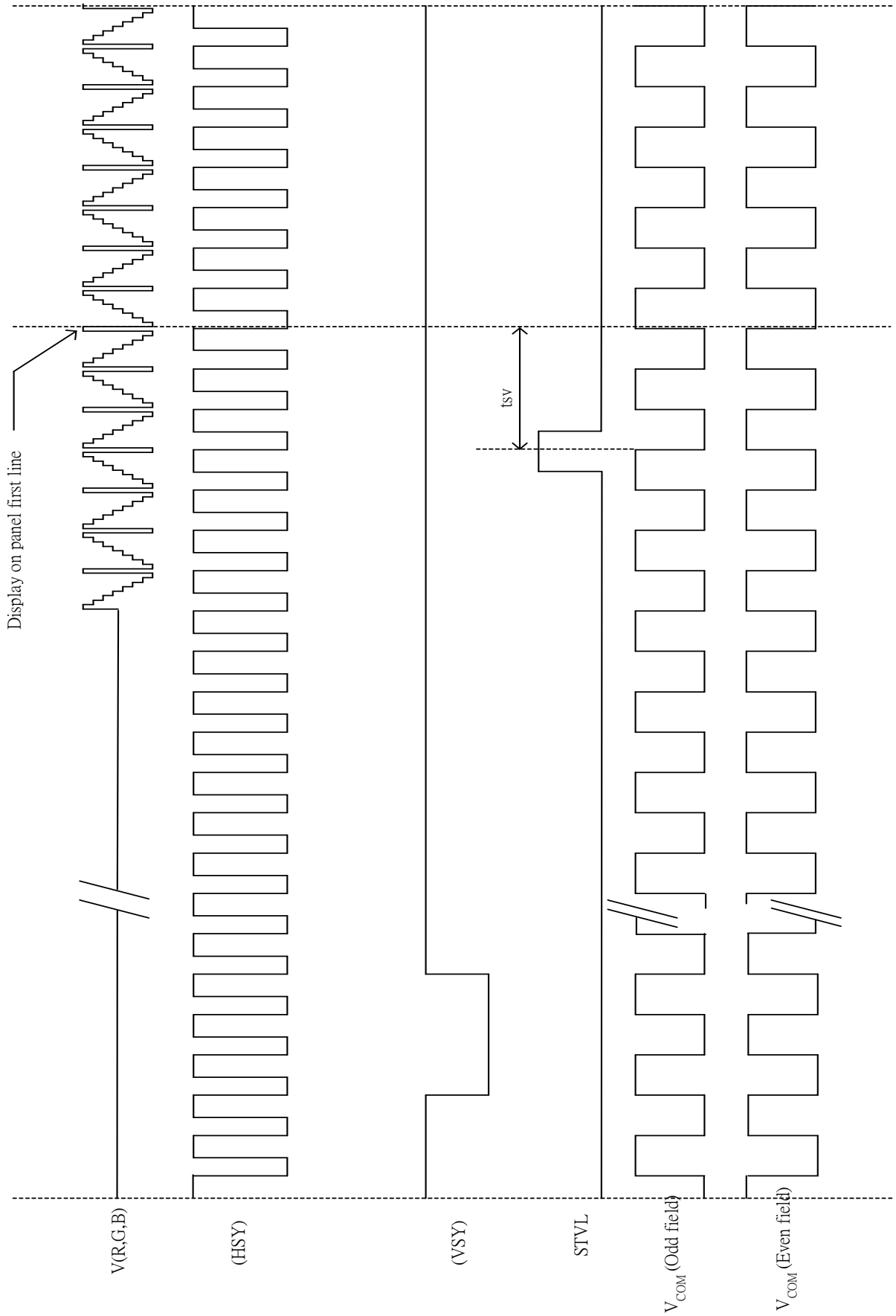


Fig. 8-5 (a) Vertical timing (From Up to Down)

Vertical timing (From down to up)

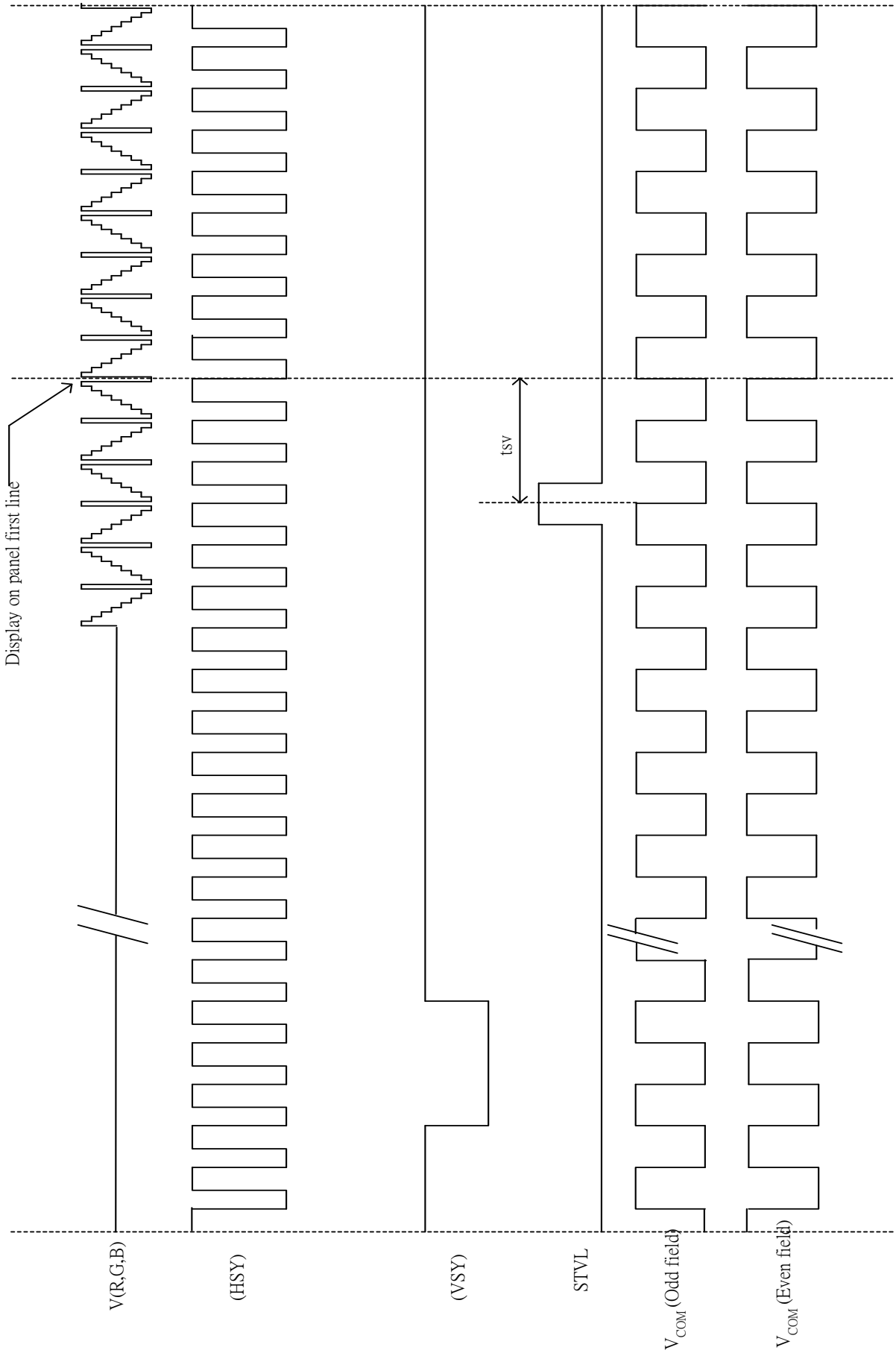
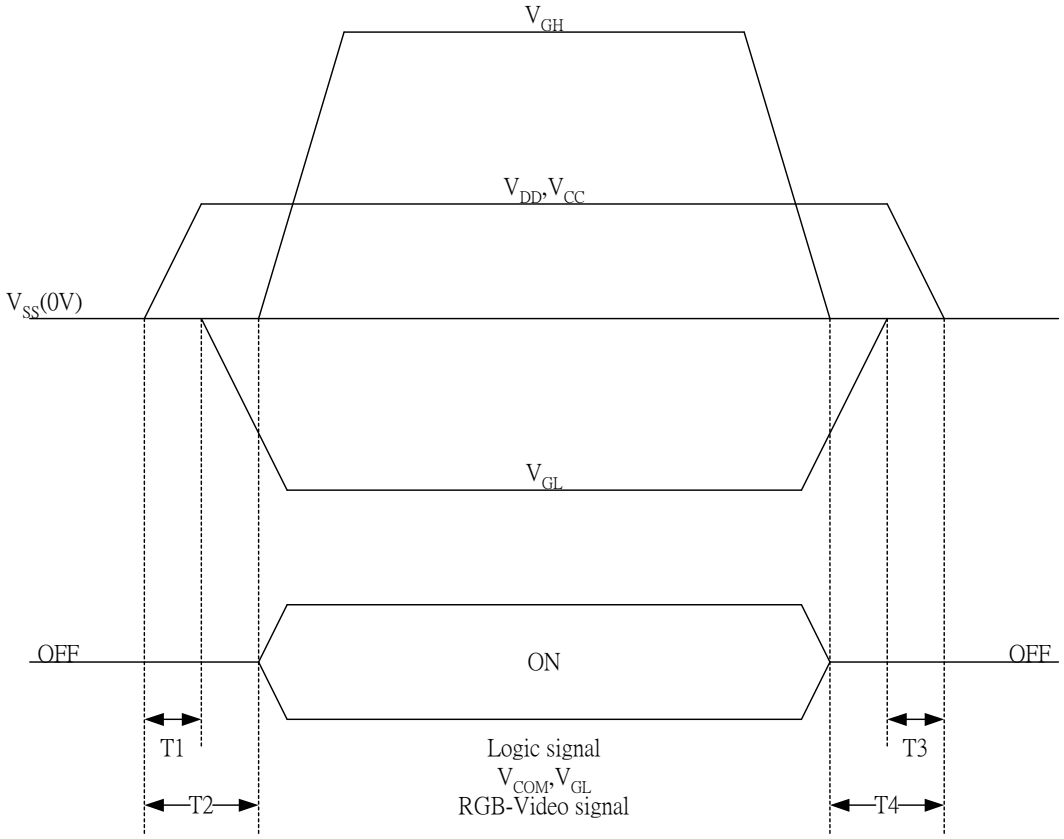


Fig. 8-5 (b) Vertical timing (From Down to Up)

9. Power on Sequence

The Power on Sequence only effect by V_{CC}, V_{DD},V_{GL} and $V_{GH,}$ the others do not care.



1) 10ms≦T1<T2
2) 0ms<T3≦T4≦10ms

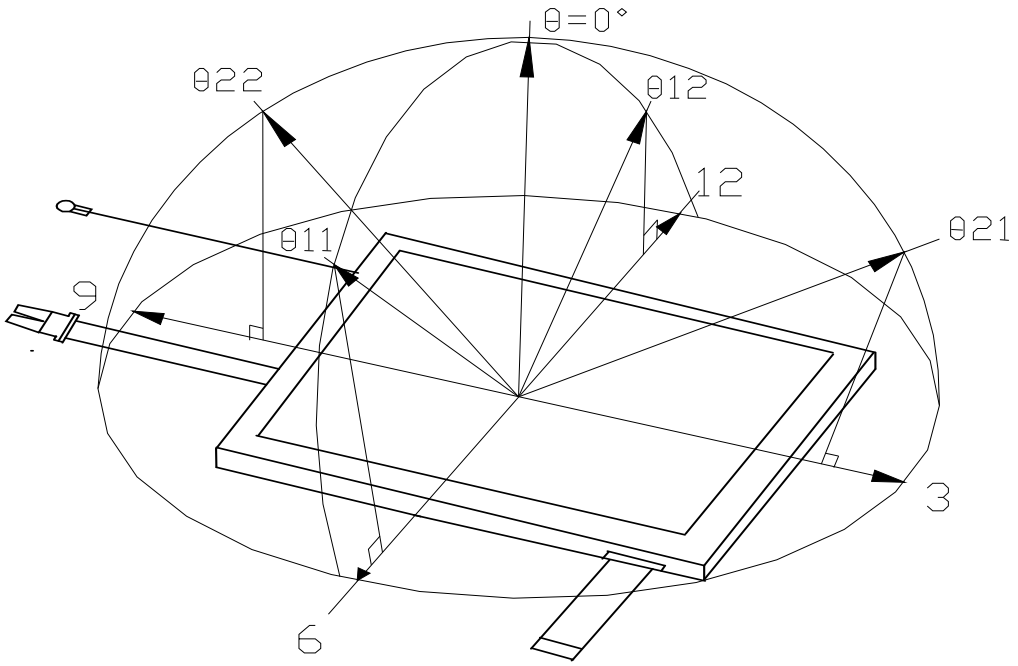
10. Optical Characteristics

10-1) Specification

Ta = 25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ21, θ22	CR≧10	45	55	-	deg	Note 10-1
	Vertical	θ12		10	15	-	deg	
		θ11		30	35	-	deg	
Contrast Ratio		CR	At optimized Viewing angle	200	350	-		Note 10-2
Response time	Rise	Tr	θ=0°		15	30	ms	Note 10-3
	Fall	Tf			25	50	ms	
Brightness		L	θ=0°	300	350		cd/㎡	Note 10-4
White Chromaticity		x	θ=0°	0.28	0.31	0.34		
		y		0.30	0.33	0.36		
Uniformity		U		70	75		%	Note 10-5
Lamp Life Time					40000		hr	

Note 10-1 : The definitions of viewing angles

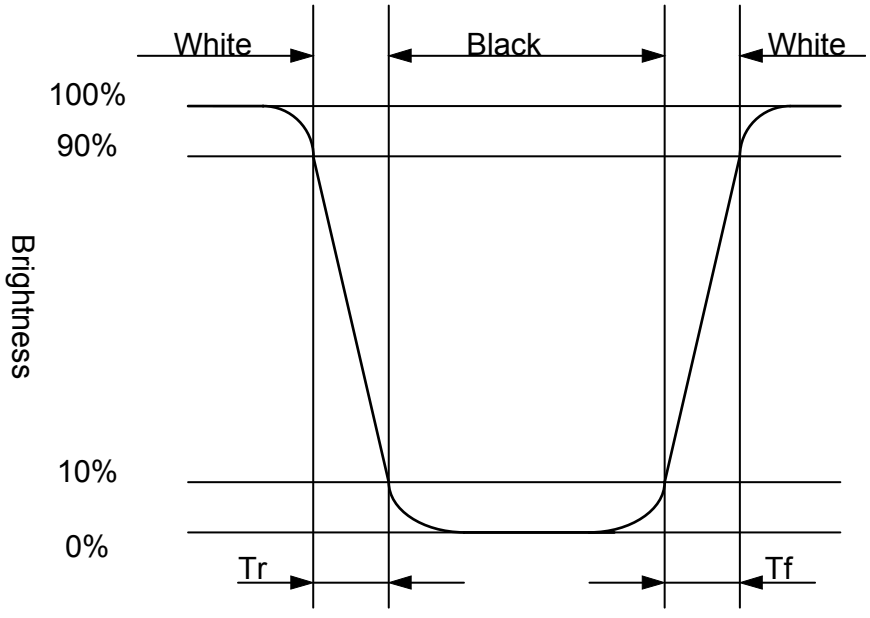


Note 10-2 : CR = $\frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

(Testing configuration see 10-2)

Contrast Ratio is measured in optimum common electrode voltage.

Note 10-3 : The definition of response time:



Note 10-4 : 1.Topcon BM-7(fast) luminance meter 1°field of view is used in the testing (after 20~30 minutes operation).

2.Lamp current : 6 mA

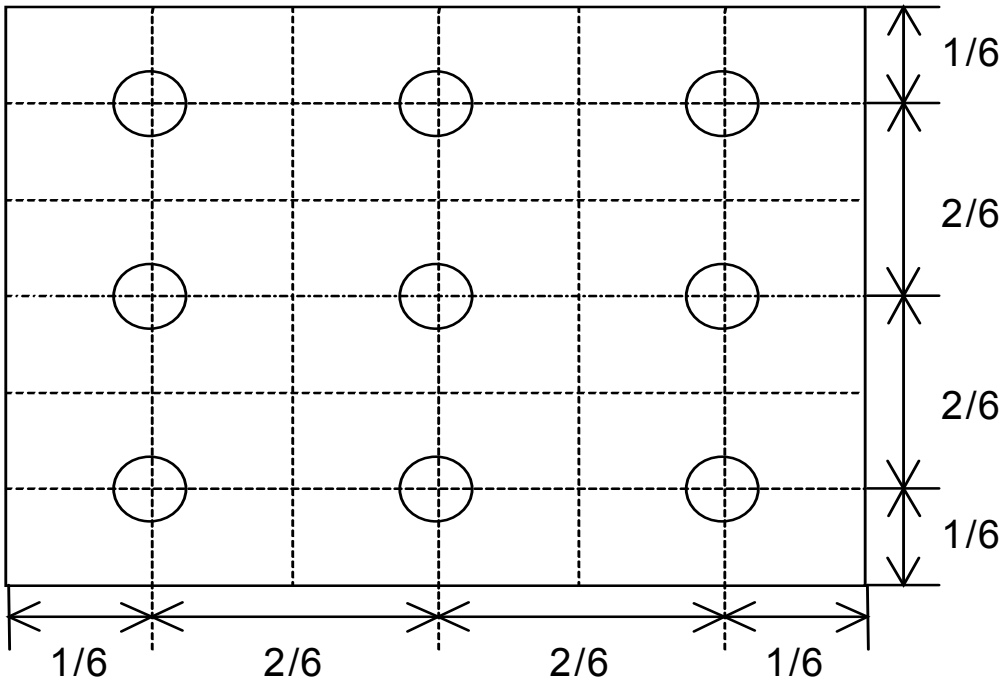
3.Inverter model : TDK-347

Note 10-5 : The uniformity of LCD is defined as

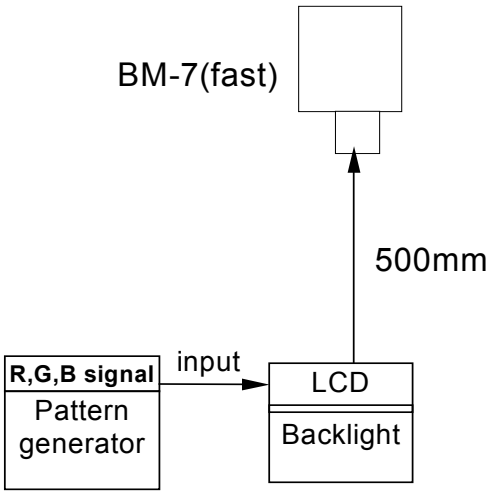
$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

Luminance meter : BM-5A or BM-7 fast (TOPCON)
Measurement distance : 500 mm +/- 50 mm
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).

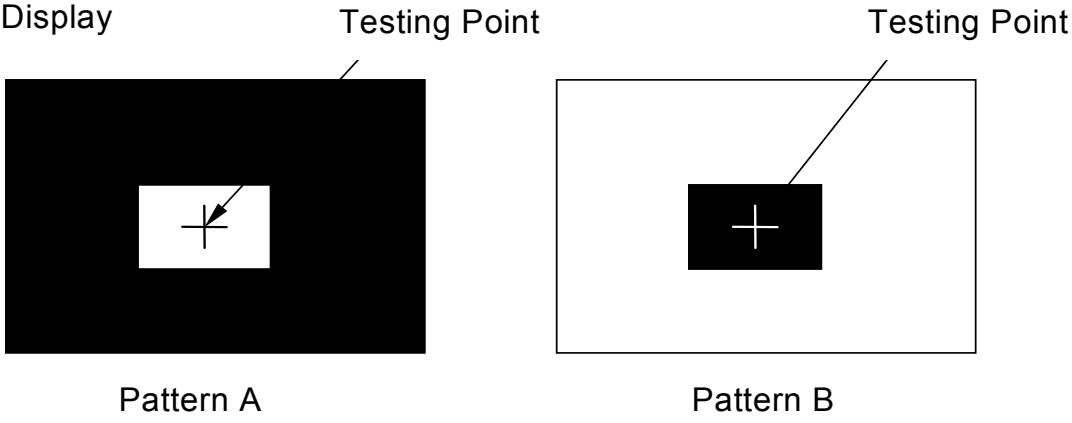


10-2) Testing configuration

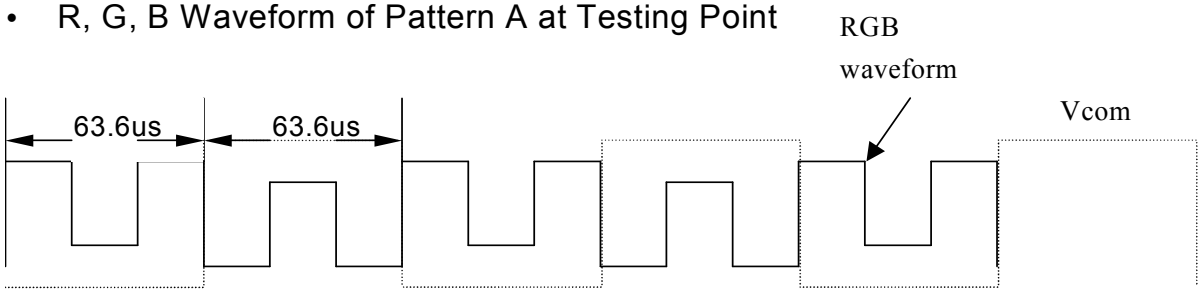


Caution: 1. Environmental illumination ≦ 1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

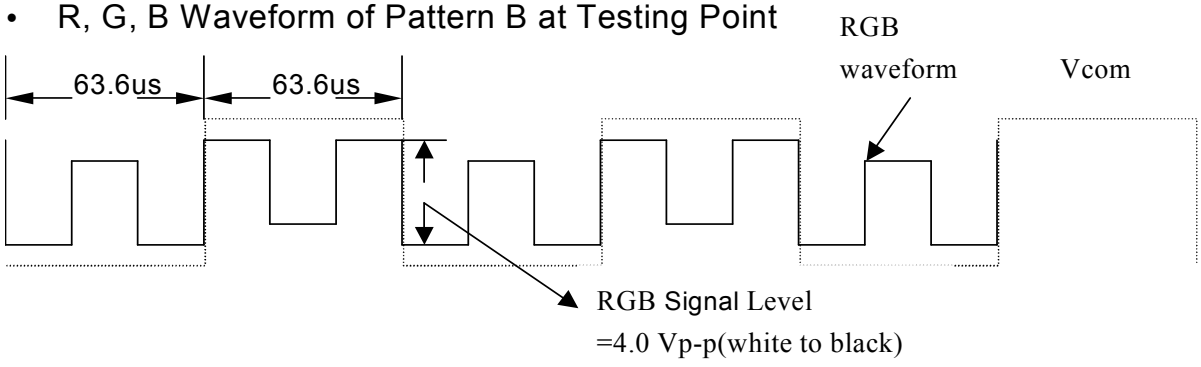
- LCD Display



- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



11. Handling Cautions

11-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.

1.The noise from the backlight unit will increase.

2.The output from inverter circuit will be unstable.

3.In some cases a part of module will heat.

c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

11-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

11-3) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

12. Reliability Test

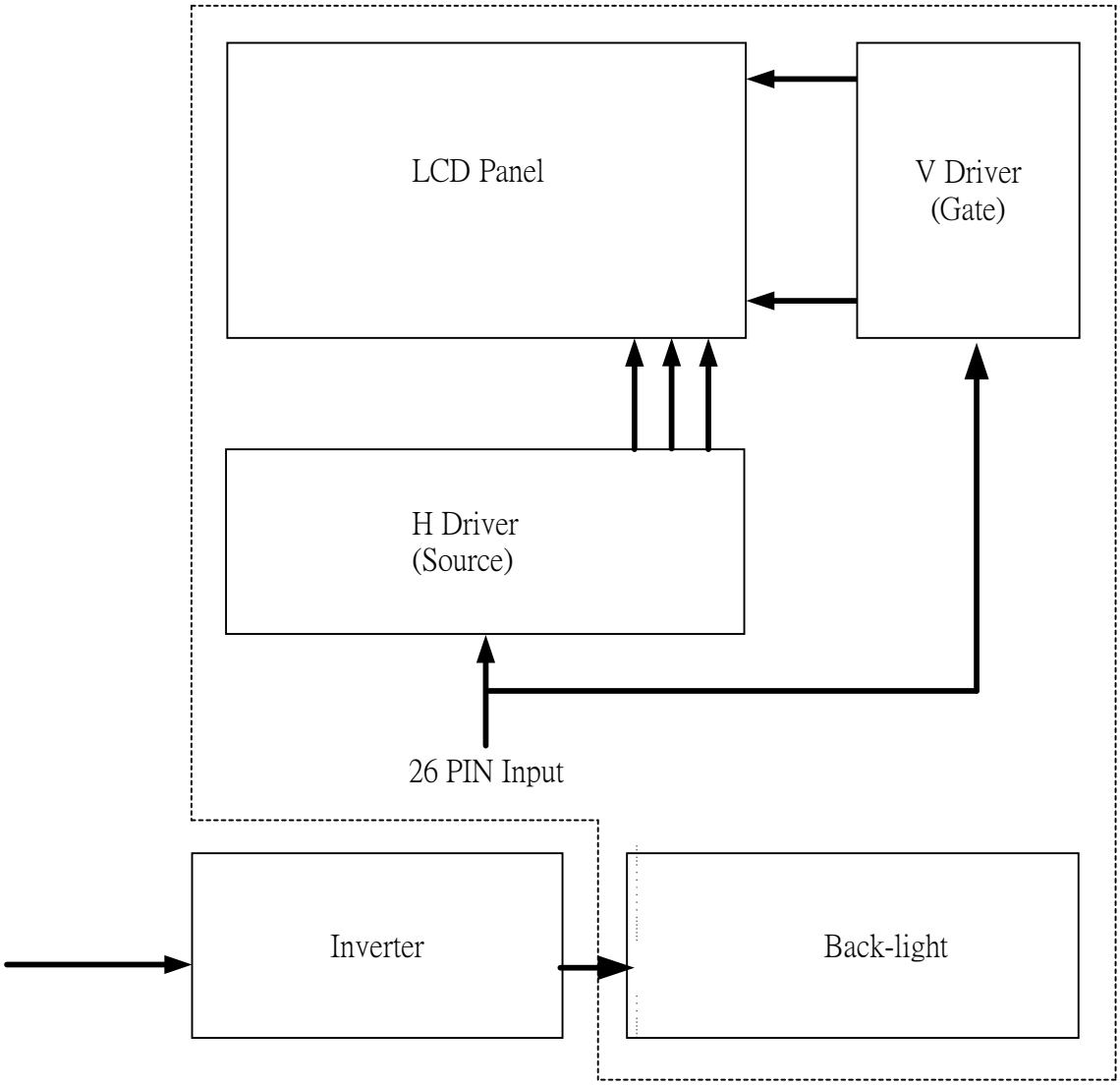
No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +70℃, 240 hrs
2	Low Temperature Storage Test	Ta = -20℃, 240 hrs
3	High Temperature Operation Test	Ta = +60℃, 240 hrs
4	Low Temperature Operation Test	Ta = 0℃, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +50℃, 80%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-20℃ → +70℃, 200 Cycles 30 min 30 min
7	Vibration Test (non-operating)	Frequency：10 ~ 55 H_Z Amplitude：1 mm Sweep time: 11 mins Test Period: 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction: ±X, ±Y, ±Z Cycle: 3 times
9	Electrostatic Discharge Test (non-operating)	200pF , 0Ω ±200V 1 time / each terminal

Ta: ambient temperature

Note : The protective film must be removed before temperature test.

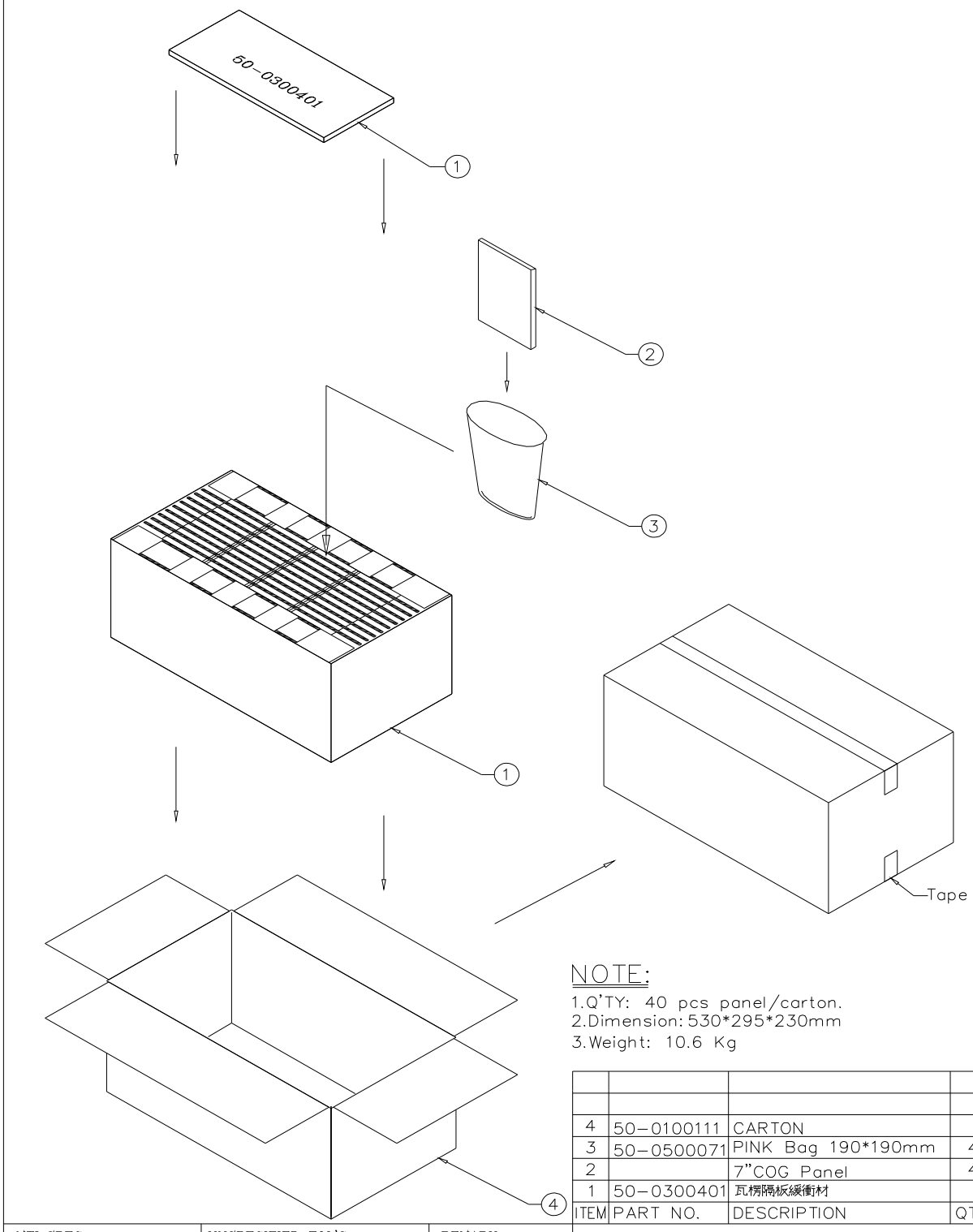
[Criteria]
Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

13. Block Diagram



14. Packing

ZONE	REV.	DOCUUMENT NO.	DESCRIPTION	DATE	REV.BY



NOTE:
1.Q'TY: 40 pcs panel/carton.
2.Dimension: 530*295*230mm
3.Weight: 10.6 Kg

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
4	50-0100111	CARTON	1	
3	50-0500071	PINK Bag 190*190mm	40	抗靜電
2		7"COG Panel	40	
1	50-0300401	瓦楞隔板緩衝材	1	上蓋+ 底座

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK	元太科技工業股份有限公司 Prime View International Co., Ltd.

			SCALE	UNIT	SHEET	DWG.TITLE
APPROVE		. .			1 OF 1	7"Hannstar Model Packing Draw
CHECK		. .				
DRAWN	CCWeng	'05.03.04	MTL.NO.		DWG FILE:	REV. 01 / A4 SIZE

Revision History

Rev.	Issued Date	Revised Contents
1.0	Mar. 08, 2005	NEW