# 3-3/4 DIGIT A/D CONVERTER WITH FREQUENCY COUNTER AND LOGIC PROBE

## FEATURES

- **Multiple Analog Measurement System**
  - **— Digit A/D Converter**
  - **— Frequency Counter**
  - **— Logic Probe**
- **Low Noise A/D Converter:**
  - **— Differential Inputs, (1pA Bias Current)**
  - **— On-Chip 50PPM/°C Voltage Reference**
- **Frequency Counter:**
  - **— 4Mhz Maximum Input Frequency**
  - **— Auto-ranging Over Four Decade Range**
- **Logic Probe:**
  - **— Two LCD Annunciators**
  - **— Buzzer Driver**
- **3-3/4 Digit Display with Overrange Indicator**
- **LCD Display Driver with Built-in Contrast Control**
- **Data Hold Input for Comparison Measurements**
- **Low Battery Detect with LCD Annunciator**
- **Underrange and Overrange Outputs**
- **On-Chip Buzzer Driver with Control Input**
- **44-Pin Plastic Flat Pack or PLCC or 40-Pin Plastic DIP Packages**
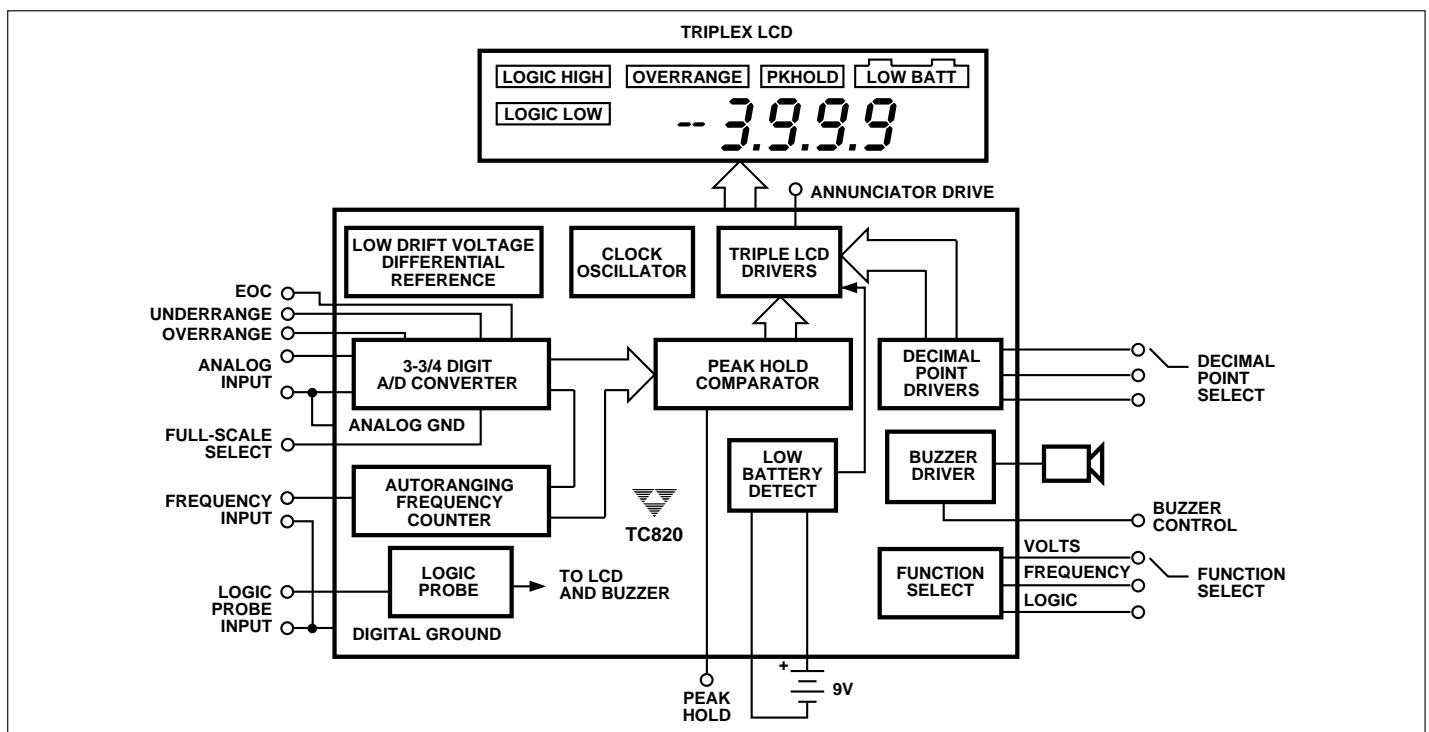
## GENERAL DESCRIPTION

The TC820 is a 3-3/4 digit, multi-measurement system especially suited for use in portable instruments. It integrates a dual slope A/D converter, auto-ranging frequency counter and logic probe into a single 44-pin surface mount or 40-pin through hole package. The TC820 operates from a single 9V input voltage (battery) and features a built-in battery low flag. Function and decimal point selection are accomplished with simple logic inputs designed for direct connection to an external microcontroller or rotary switch.

Ease of use, low power operation and high functional integration make the TC820 desirable in a variety of analog measurement applications.

## ORDERING INFORMATION

| Part No. | Resolution | Package | Temperature Range |
|---|---|---|---|
| TC820CKW | 3-3/4 Digits | 44-Pin Plastic Quad Flat Package | 0°C to +70°C |
| TC820CLW | 3-3/4 Digits | 44-Pin Plastic Leadless Chip Carrier | 0°C to +70°C |
| TC820CPL | 3-3/4 Digits | 40-Pin Plastic DIP | 0°C to +70°C |

## FUNCTIONAL BLOCK DIAGRAM

# TC820

## GENERAL DESCRIPTION

The TC820 is a 3-3/4 digit measurement system combining an integrating analog-to-digital converter, frequency counter, and logic level tester in a single package. The TC820 supersedes the TC7106 in new designs by improving performance and reducing system cost. The TC820 adds features that are difficult, expensive, or impossible to provide with older A/D converters (see the competitive evaluation). The high level of integration permits TC820-based instruments to deliver higher performance and more features, while actually reducing parts count. Fabricated in low-power CMOS, the TC820 directly drives a 3-3/4 digit (3999 maximum) LCD.

With a maximum range of 3999 counts, the TC820 provides 10 times greater resolution in the 200mV to 400mV range than traditional 3-1/2 digit meters. An auto-zero cycle guarantees a zero reading with a 0V input. CMOS processing reduces analog input bias current to only 1pA. Rollover error (the difference in readings for equal magnitude but opposite polarity input signals) is less than ±1 count. Differential reference inputs permit ratiometric measurements for ohms or bridge transducer applications.

The TC820's frequency counter option simplifies design of an instrument well-suited to both analog and digital troubleshooting: voltage, current, and resistance measurements, plus precise frequency measurements to 4MHz (higher frequencies can be measured with an external prescaler), and a simple logic probe. The frequency counter will automatically adjust its range to match the input frequency, over a four-decade range.

Two logic level measurement inputs permit a TC820-based meter to function as a logic probe. When combined with external level shifters, the TC820 will display logic levels on the LCD and also turn on a piezoelectric buzzer when the measured logic level is low.

Other TC820 features simplify instrument design and reduce parts count. On-chip decimal point drivers are included, as is a low battery detection annunciator. A piezoelectric buzzer can be controlled with an external switch or by the logic probe inputs. Two oscillator options are provided: A crystal can be used if high accuracy frequency measurements are desired, or a simple RC option can be used for low-end instruments.

A "peak reading hold" input allows the TC820 to retain the highest A/D or frequency reading. This feature is useful in measuring motor starting current, maximum temperature, and similar applications.

A family of instruments can be created with the TC820. No additional design effort is required to create instruments with 3-3/4 digit resolution.

The TC820 operates from a single 9V battery, with typical power of 10 mW. Packages include a 40-pin plastic DIP, 44-pin plastic flat package, and 44-pin PLCC.

## COMPETITIVE EVALUATION

| Features Comparison | TC820 | 7106 |
|---|---|---|
| 3-3/4 Digit Resolution | Yes | No |
| Auto-Ranging Frequency Counter | Yes | No |
| Logic Probe | Yes | No |
| Decimal Point Drive | Yes | No |
| Peak Reading Hold (Frequency or Voltage) | Yes | No |
| Display Hold | Yes | No |
| Simple 10:1 Range Change | Yes | No |
| Buzzer Drive | Yes | No |
| Low Battery Detection With Annunciator | Yes | No |
| Overrange Detection With Annunciator | Yes | No |
| Low Drift Reference | Yes | No |
| Underrange/Overrange Logic Output | Yes | No |
| Input Overload Display | "OL" | "1" |
| LCD Annunciator Driver | Yes | No |
| LCD Drive Type | Triplexed | Direct |
| LCD Pin Connections | 15 | 24 |
| LCD Elements | 36 | 23 |

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# 3-3/4 DIGIT A/D CONVERTER WITH FREQUENCY AND LOGIC PROBE

## ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ($V_{DD}$ to GND) ...................................... 15V
Analog Input Voltage (Either Input) (Note 1) .... $V_{DD}$ to $V_{SS}$
Reference Input Voltage (Either Input) ............. $V_{DD}$ to $V_{SS}$
Digital Inputs .............................................. $V_{DD}$ to DGND
$V_{DISP}$ .......................................... $V_{DD}$ to (DGND − 0.3V)
Package Power Dissipation ($T_A \leq 70°C$) (Note 2)
    40-Pin Plastic DIP ............................................. 1.23W
    44-Pin PLCC ...................................................... 1.23W
    44-Pin Plastic Flat Package .............................. 1.00W
Operating Temperature Range
    "C" Devices ........................................... 0°C to +70°C
    "E" Devices ..................................... − 40°C to +85°C
Storage Temperature Range ................ − 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ................... 300°C

*Static-sensitive devices. Unused devices should be stored in conductive material to protect against static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**NOTES:** 1. Input voltages may exceed the supply voltages provided that input current is limited to ±100µA. Current above this value may result in invalid display readings but will not destroy the device if limited to ±1mA.
2. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

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## ELECTRICAL CHARACTERISTICS: $V_S$ = 9V, $T_A$ = 25°C, unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Zero Input Reading | $V_{IN}$ = 0V<br>Full Scale = 400 mV | − 000 | ±000 | +000 | Digital Reading |
| RE | Roll-Over Error | $V_{IN}$ = ±390mV<br>Full-Scale = 400mV | − 1 | ±0.2 | +1 | Counts |
| NL | Nonlinearity (Maximum Deviation From Best Straight Line Fit) | Full-Scale = 400mV | − 1 | ±0.2 | +1 | Count |
| | Ratiometric Reading | $V_{IN}$ = $V_{REF}$, TC820 | 1999 | 1999/2000 | 2000 | Digital |
| CMRR | Common-Mode Rejection Ratio | $V_{CM}$ = ±1V, $V_{IN}$ = 0V<br>Full-Scale = 400mV<br>($V_{FS}$ = 200 mV) | — | 50 | — | µV/V |
| VCMR | Common-Mode Voltage Range | Input High, Input Low | $V_{SS}$ + 1.5 | — | $V_{DD}$− 1 | V |
| $e_N$ | Noise (P-P Value Not Exceeded 95% of Time) | $V_{IN}$ = 0V<br>Full-Scale = 400mV | — | 15 | — | µV |
| $I_{IN}$ | Input Leakage Current | $V_{IN}$ = 0V<br>$T_A$ = 25°C<br>0°C ≤ $T_A$ ≤ +70°C<br>− 40°C ≤ $T_A$ ≤ +85°C | —<br>—<br>— | 1<br>20<br>100 | 10<br>—<br>— | pA |
| $V_{COM}$ | Analog Common Voltage | 25 kΩ Between Common and $V_{DD}$<br>($V_{SS}$ − $V_{COM}$) | 3.15 | 3.3 | 3.45 | V |
| $V_{CTC}$ | Common Voltage Temperature Coefficient | 25 kΩ Between Common and $V_{DD}$<br>0°C ≤ $T_A$ ≤ +70°C<br>− 40°C ≤ $T_A$ ≤ +85°C | —<br>— | 35<br>50 | 50<br>— | ppm/°C |
| $TC_{ZS}$ | Zero Reading Drift | $V_{IN}$ = 0V<br>0°C ≤ $T_A$ ≤ +70°C<br>− 40°C ≤ $T_A$ ≤ +85°C | —<br> | 0.2<br>1 | —<br> | µV/°C |
| $TC_{FS}$ | Scale Factor Temperature Coefficient | $V_{IN}$ = 399mV<br>0°C ≤ $T_A$ ≤ +70°C<br>− 40°C ≤ $T_A$ ≤ +85°C<br>Ext Ref = 0 ppm/°C | —<br>— | 1<br>5 | 5<br>— | ppm/°C |
| $I_S$ | Supply Current | $V_{IN}$ = 0V | — | 1 | 1.5 | mA |
| | Peak-to-Peak Backplane Drive Voltage | $V_S$ = 9V<br>$V_{DISP}$ = DGND | 4.25 | 4.7 | 5.3 | V |

# TC820

## ELECTRICAL CHARACTERISTICS (Cont.)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
| | Buzzer Frequency | $f_{OSC}$ = 40kHz | — | 5 | — | kHz |
| | Counter Timebase Period | $f_{OSC}$ = 40kHz | — | 1 | — | Second |
| | Low Battery Flag Voltage | $V_{DD}$ to $V_{SS}$ | 6.7 | 7 | 7.3 | V |
| $V_{IL}$ | Input Low Voltage | | — | — | DGND + 1.5 | V |
| $V_{IH}$ | Input High Voltage | | $V_{DD}$ – 1.5 | — | — | V |
| $V_{OL}$ | Output Low Voltage, UR, OR Outputs | $I_L$ = 50µA | — | — | DGND + 0.4 | V |
| $V_{OL}$ | Output High Voltage, UR, OR Outputs | $I_L$ = 50µA | $V_{DD}$ – 1.5 | — | — | V |
| | Control Pin Pull-Down Current | $V_{IN}$ = $V_{DD}$ | — | 5 | — | µA |

## PIN DESCRIPTION

| Pin No. (40-Pin Package) | Pin No. (44-Pin Flat Package) | Symbol | Description |
|--------------------------|-------------------------------|--------|-------------|
| 1 | 40 | L-E4 | LCD segment driver for L ("logic LOW"), polarity, and "e" segment of most significant digit (MSD). |
| 2 | 41 | AGD4 | LCD segment drive for "a," "g," and "d" segments of MSD. |
| 3 | 42 | BC4P3 | LCD segment drive for "b" and "c" segments of MSD and decimal point 3. |
| 4 | 43 | HFE3 | LCD segment drive for H ("logic HIGH"), and "f" and "e" segments of third LSD. |
| 5 | 44 | AGD3 | LCD segment drive for "a," "g," and "d" segments of third LSD. |
| 6 | 1 | BC3P2 | LCD segment drive for "b" and "c" segments of third LSD and decimal point 2. |
| 7 | 2 | OFE2 | LCD segment drive for "overrange," and "f" and "e" segments of second LSD. |
| 8 | 3 | AGD2 | LCD segment drive for "a," "g," and "d" segments of second LSD. |
| 9 | 4 | BC2P1 | LCD segment drive for "b " and "c" segments of second LSD and decimal point 1. |
| 10 | 5 | PKFE1 | LCD segment drive for "hold peak reading," and "f" and "e" segments of LSD. |
| 11 | 6 | AGD1 | LCD segment drive for "a," "g," and "d" segments of LSD. |
| 12 | 7 | BC1BT | LCD segment drive for "b" and "c" segments of LSD and "low battery." |
| 13 | 8 | BP3 | LCD backplane #3. |
| 14 | 9 | BP2 | LCD backplane #2. |
| 15 | 10 | BP1 | LCD backplane #1. |
| — | 11 | $V_{DISP}$ | Sets peak LCD drive signal: $V_{PEAK}$ = ($V_{DD}$) – $V_{DISP}$. $V_{DISP}$ may also be used to compensate for temperature variation of LCD crystal threshold voltage. |
| 16 | 12 | DGND | Internal logic digital ground, the logic "0" level. Nominally 4.7V below $V_{DD}$. |
| 17 | 13 | ANNUNC | Square-wave output at the backplane frequency, synchronized to BP1. ANNUNC can be used to control display annunciators. Connecting an LCD segment to ANNUNC turns it on; connecting it to its backplane turns it off. |
| 18 | 14 | LOGIC | Logic mode control input. When connected to $V_{DD}$, the converter is in logic mode. The LCD displays "OL" and the decimal point inputs control the HIGH and LOW annunciators. When the "low" annunciator is on, the buzzer will also be on. When unconnected or connected to DGND, the TC820 is in the voltage/frequency measurement mode. This pin has a 5µA internal pull-down to DGND. |
| 19 | 15 | RANGE/ FREQ | Dual-purpose input. In range mode, when connected to $V_{DD}$, the integration time will be 200 counts instead of 2000 counts and the LCD will display the analog input divided by 10. (See text for limitation with TC820.) In frequency mode, this pin is the frequency input. A digital signal applied to this pin will be measured with a 1-second time base. There is an internal 5µA pull-down to DGND. |

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## PIN DESCRIPTION

| Pin No. (40-Pin Package) | Pin No. (44-Pin Flat Package) | Symbol | Description |
|---|---|---|---|
| 20 | 16 | DP0/LO | Dual-purpose input. Decimal point select input for voltage measurements. In logic mode, connecting this pin to $V_{DD}$ will turn on the "low" LCD segment. There is an internal 5µA pull-down to DGND in volts mode only. Decimal point logic:<br><br>DP1 DP0 Decimal Point Selected<br>0 0 None<br>0 1 DP1<br>1 0 DP2<br>1 1 DP3 |
| 21 | 17 | DP1/HI | Dual-purpose input. Decimal point select input for voltage measurements. In logic mode, connecting this pin to $V_{DD}$ will turn on the "high" LCD segment. There is an internal 5µA pull-down to DGND in volts mode only. |
| 22 | 18 | BUZOUT | Buzzer output. Audio frequency, 5kHz, output which drives a piezoelectric buzzer. |
| 23 | 19 | BUZIN | Buzzer control input. Connecting BUZIN to $V_{DD}$ turns the buzzer on. BUZIN is logically ORed (internally) with the "logic level low" input. There is an internal 5µA pull-down to DGND. |
| 24 | 20 | $\overline{FREQ}$/ $\overline{VOLTS}$ | Voltage or frequency measurement select input. When unconnected, or connected to DGND, the A/D converter function is active. When connected to $V_{DD}$, the frequency counter function is active. This pin has an internal 5µA pull-down to DGND. |
| 25 | 21 | PKHOLD | Peak hold input. When connected to $V_{DD}$, the converter will only update the display if a new conversion value is greater than the preceding value. Thus, the peak reading will be stored and held indefinitely. When unconnected, or connected to DGND, the converter will operate normally. This pin has an internal 5µA pull-down to DGND. |
| | 22 | UR | Underrange output. This output will be HIGH when the digital reading is 380 counts or less. |
| | 23 | OR | Overrange output. This output will be HIGH when the analog signal input is greater than full scale. The LCD will display "OL" when the input is overranged. |
| 26 | 24 | $V_{SS}$ | Negative supply connection. Connect to negative terminal of 9V battery. |
| 27 | 25 | COM | Analog circuit ground reference point. Nominally 3.3V below $V_{DD}$. |
| 28 | 26 | $C_{REF}^+$ | Positive connection for reference capacitor. |
| 29 | 27 | $C_{REF}^-$ | Negative connection for reference capacitor. |
| 30 | 28 | $V_{REF}^+$ | High differential reference input connection. |
| 31 | 29 | $V_{REF}^-$ | Low differential reference input connection. |
| 32 | 30 | $V_{IN}^-$ | Low analog input signal connection. |
| 33 | 31 | $V_{IN}^+$ | High analog input signal connection. |
| 34 | 32 | $V_{BUFF}$ | Buffer output. Connect to integration resistor. |
| 35 | 33 | $C_{AZ}$ | Auto-zero capacitor connection. |
| 36 | 34 | $V_{INT}$ | Integrator output. Connect to integration capacitor. |
| | 35 | $\overline{EOC}$/ HOLD | Bidirectional pin. Pulses low (i.e., from $V_{DD}$ to DGND) at the end of each conversion. If connected to $V_{DD}$, conversions will continue, but the display is not updated. |
| 37 | 36 | OSC1 | Crystal oscillator (input) connection. |
| 38 | 37 | OSC2 | Crystal oscillator (output) connection. |
| 39 | 38 | OSC3 | RC oscillator connection. |
| 40 | 39 | $V_{DD}$ | Positive power supply connection, typically 9V. |

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## PIN CONFIGURATIONS



**TC820CPL**

| Pin | Signal | | Pin | Signal |
|---|---|---|---|---|
| SEGMENTS L-E4 | 1 | | 40 | $V_{DD}$ |
| SEGMENTS AGD4 | 2 | | 39 | OSC3 |
| SEGMENTS BC4P3 | 3 | | 38 | OSC2 |
| SEGMENTS HFE3 | 4 | | 37 | OSC1 |
| SEGMENTS AGD3 | 5 | | 36 | $V_{INT}$ |
| SEGMENTS BC3P2 | 6 | | 35 | $C_{AZ}$ |
| SEGMENTS OFE2 | 7 | | 34 | $V_{BUFF}$ |
| SEGMENTS AGD2 | 8 | | 33 | $V_{IN}^{+}$ |
| SEGMENTS BCP1 | 9 | | 32 | $V_{IN}^{-}$ |
| SEGMENTS PKFE1 | 10 | | 31 | $V_{REF}^{-}$ |
| SEGMENTS AGD1 | 11 | | 30 | $V_{REF}^{+}$ |
| SEGMENTS BC1BT | 12 | | 29 | $C_{REF}^{-}$ |
| BP3 | 13 | | 28 | $C_{REF}^{+}$ |
| BP2 | 14 | | 27 | COM |
| BP1 | 15 | | 26 | $V_{SS}$ |
| DGND | 16 | | 25 | PK HOLD |
| ANNUNC | 17 | | 24 | $\overline{FREQ/VOLTS}$ |
| LOGIC | 18 | | 23 | BUZ IN |
| RANGE/FREQ | 19 | | 22 | BUZ OUT |
| DP0/LO | 20 | | 21 | DP1/HI |

**TC820CLW**

Top pins (left to right): AGD3 (6), HFE3 (5), BC4P3 (4), AGD4 (3), L-E4 (2), $V_{DD}$ (1), OSC3 (44), OSC2 (43), OSC1 (42), $\overline{EOC/HOLD}$ (41), $V_{INT}$ (40)

Left pins: BC3P2 (7), OFE2 (8), AGD2 (9), BC2P1 (10), PKFE1 (11), AGD1 (12), BP1BT (13), BP3 (14), BP2 (15), BP1 (16), $V_{DISP}$ (17)

Right pins: $C_{AZ}$ (39), $V_{BUFF}$ (38), $V_{IN}^{+}$ (37), $V_{IN}^{-}$ (36), $V_{REF}^{-}$ (35), $V_{REF}^{+}$ (34), $C_{REF}^{-}$ (33), $C_{REF}^{+}$ (32), COM (31), $V_{SS}$ (30), OR (29)

Bottom pins (left to right): DGND (18), ANNUNC (19), LOGIC (20), RANGE/FREQ (21), DP0/LO (22), DP1/HI (23), BUZ OUT (24), BUZ IN (25), $\overline{FREQ/VOLTS}$ (26), PK HOLD (27), UR (28)

**TC820CKW**

Top pins (left to right): AGD3 (44), HFE3 (43), BC4P3 (42), AGD4 (41), L-E4 (40), $V_{DD}$ (39), OSC3 (38), OSC2 (37), OSC1 (36), $\overline{EOC/HOLD}$ (35), $V_{INT}$ (34)

Left pins: BC3P2 (1), OFE2 (2), AGD2 (3), BCP2P1 (4), PKFE1 (5), AGD1 (6), BP1BT (7), BP3 (8), BP2 (9), BP1 (10), $V_{DISP}$ (11)

Right pins: $C_{AZ}$ (33), $V_{BUFF}$ (32), $V_{IN}^{+}$ (31), $V_{IN}^{-}$ (30), $V_{REF}^{-}$ (29), $V_{REF}^{+}$ (28), $C_{REF}^{-}$ (27), $C_{REF}^{+}$ (26), COM (25), $V_{SS}$ (24), OR (23)

Bottom pins (left to right): DGND (12), ANNUNC (13), LOGIC (14), RANGE/FREQ (15), DP0/LO (16), DP1/HI (17), BUZ OUT (18), BUZ IN (19), FREQ/VOLTS (20), PK HOLD (21), UR (22)

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# 3-3/4 A/D CONVERTER WITH
# FREQUENCY COUNTER
# AND LOGIC PROBE

## TC820

**FUNCTIONAL BLOCK DIAGRAM**



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**Figure 1. Typical Operating Circuit**
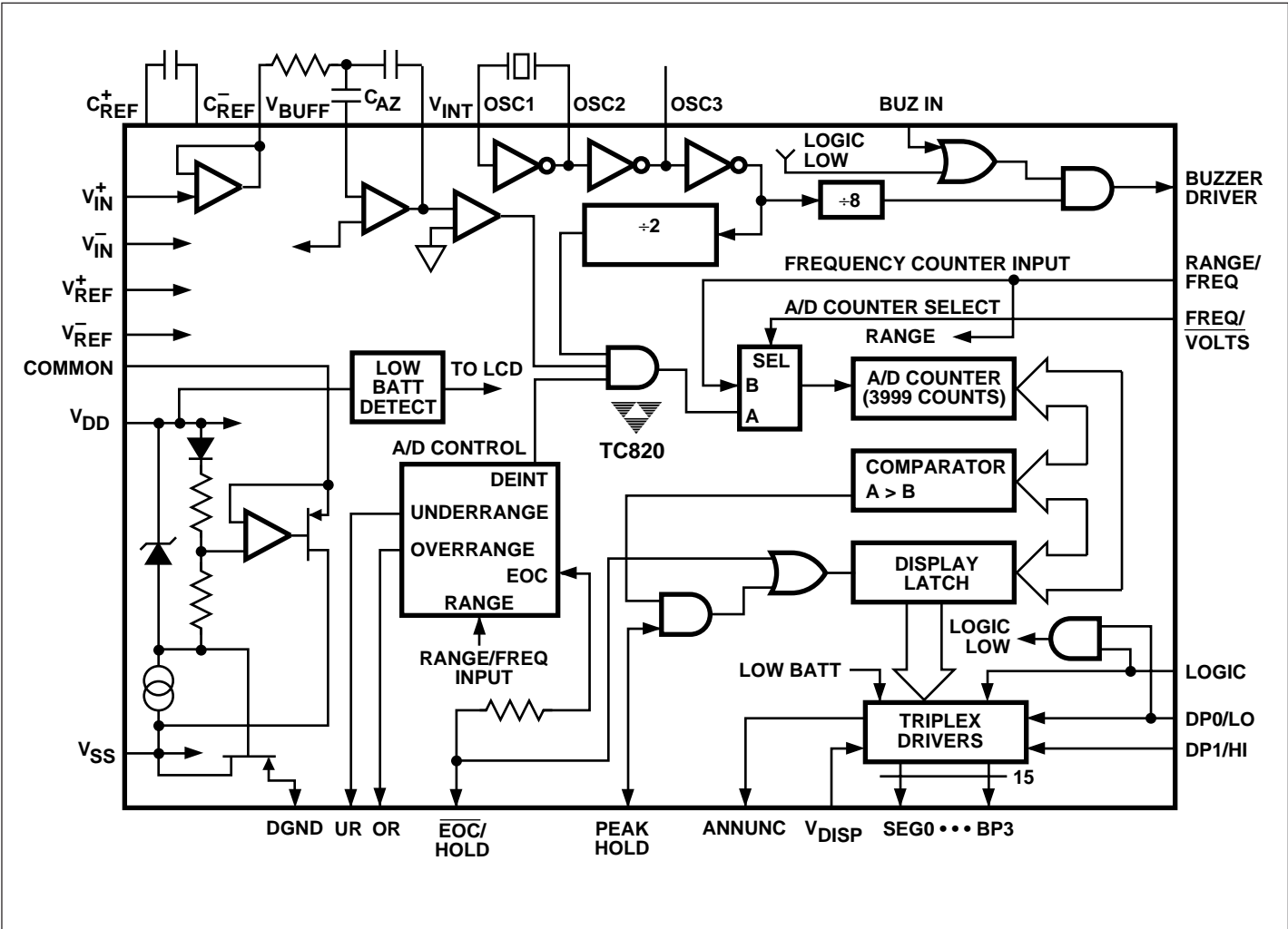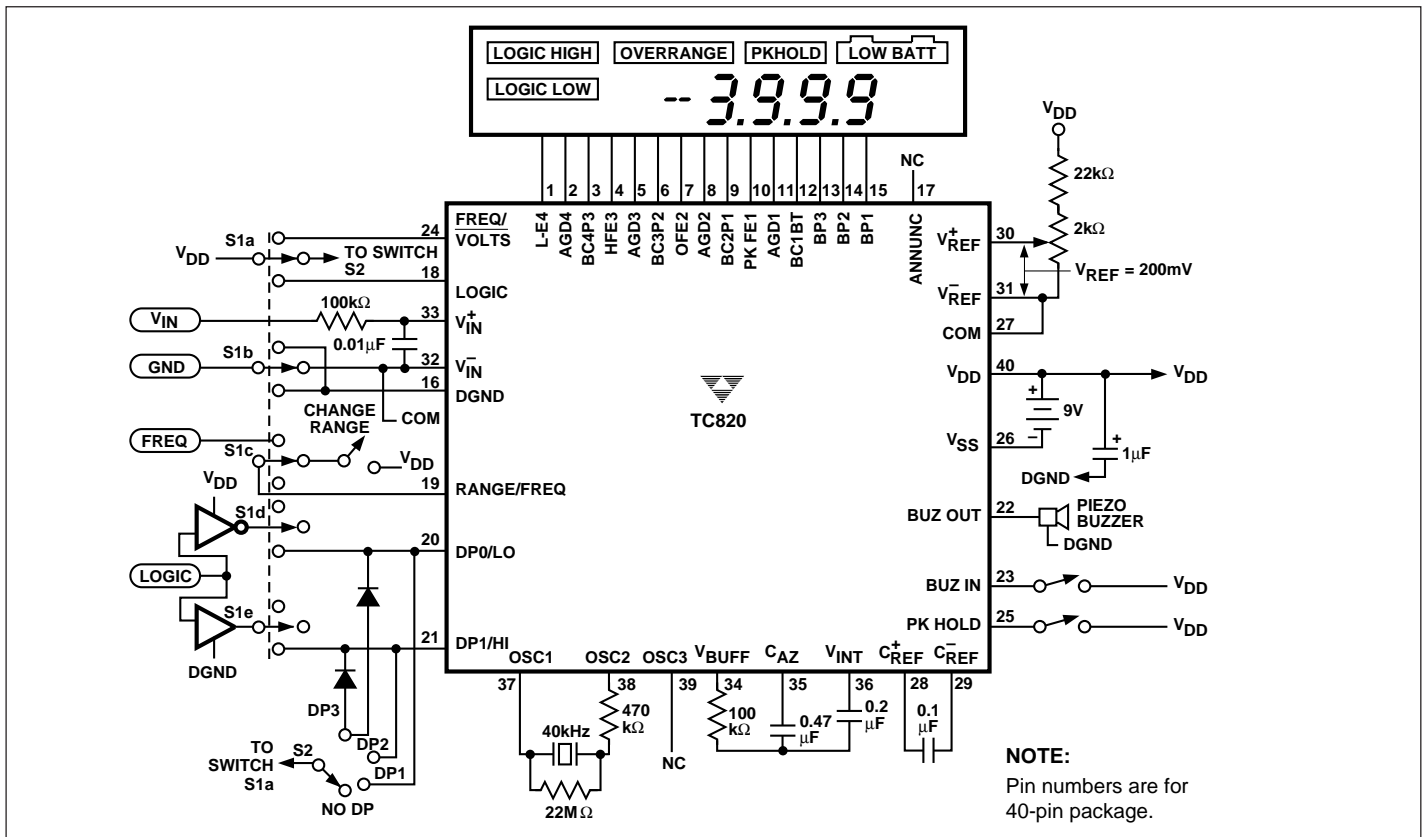
## GENERAL THEORY OF OPERATION

### Dual-Slope Conversion Principles

The TC820 analog-to-digital converter operates on the principle of dual-slope integration. An understanding of the dual-slope conversion technique will aid the user in following the detailed TC820 theory of operation following this section. A conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input Signal Integration
(2) Reference Voltage Integration (Deintegration)

Referring to Figure 2, the unknown input signal to be converted is integrated from zero for a fixed time period ($t_{INT}$), measured by counting clock pulses. A constant reference voltage of the opposite polarity is then integrated until the integrator output voltage returns to zero. The reference integration (deintegration) time ($T_{DEINT}$) is then directly proportional to the unknown input voltage ($V_{IN}$).

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" from zero and "ramp-down" back to zero. A simple mathematical equation relates the input signal, reference voltage, and integration time:



**Figure 2. Basic Dual-Slope Converter**

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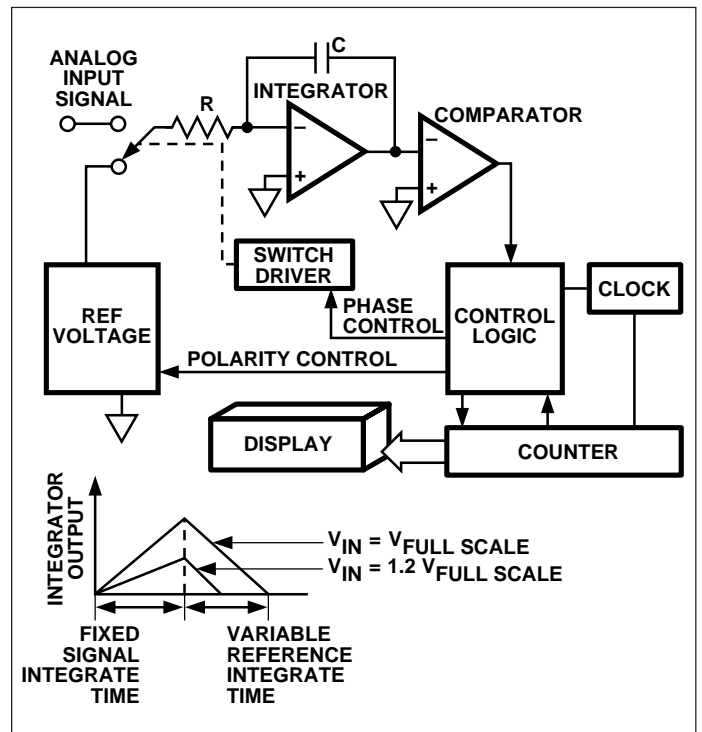
$$\frac{1}{R_{INT} C_{INT}} \int_0^{t_{INT}} V_{IN}(t)\, dt = \frac{V_{REF}\, t_{DEINT}}{R_{INT} C_{INT}}$$

where:  $V_{REF}$ = Reference voltage
$t_{INT}$ = Integration time
$t_{DEINT}$ = Deintegration time

For a constant $t_{INT}$:

$$V_{IN} = V_{REF} \times \frac{t_{DEINT}}{t_{INT}}$$

Accuracy in a dual-slope converter is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit of the dual-slope technique is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods, making integrating ADCs immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals, with frequency components at multiples of the averaging (integrating) period, will be attenuated (Figure 3). Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60Hz power line period.
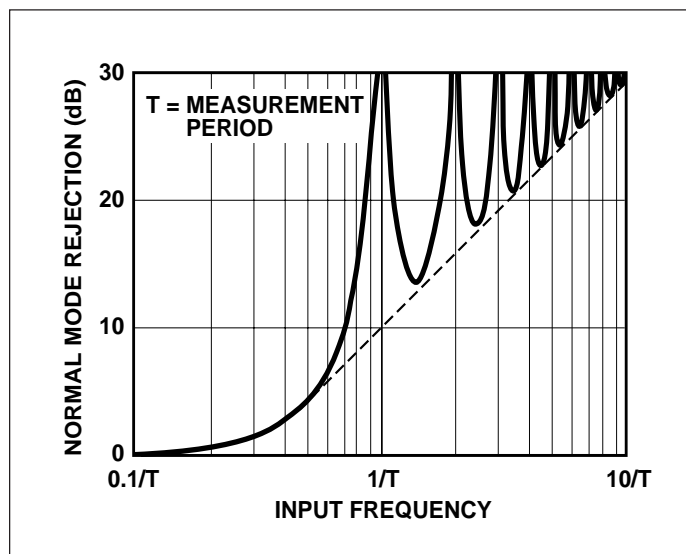


**Figure 3.  Normal-Mode Rejection of Dual-Slope Converter**

## Analog Section

In addition to the basic integrate and deintegrate dual-slope phases discussed above, the TC820 design incorporates a "zero integrator output" phase and an "auto-zero" phase. These additional phases ensure that the integrator starts at 0V (even after a severe overrange conversion), and that all offset voltage errors (buffer amplifier, integrator and

comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

(1) Zero Integrator Output
(2) Auto-Zero
(3) Signal Integrate
(4) Reference Deintegrate

### Zero Integrator Output Phase

This phase guarantees that the integrator output is at 0V before the system zero phase is entered, ensuring that the true system offset voltages will be compensated for even after an overrange conversion. The duration of this phase is 500 counts plus the unused deintegrate counts.

### Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the measurement circuit by opening internal analog switches, and the internal nodes are shorted to Analog Common ($0V_{REF}$) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit comparator offset voltage error compensation. A voltage established on $C_{AZ}$ then compensates for internal device offset voltages during the measurement cycle. The auto-zero phase residual is typically 10μV to 15μV. The auto-zero duration is 1500 counts.

### Signal Integration Phase

Upon completion of the auto-zero phase, the auto-zero loop is opened and the internal differential inputs connect to $V_{IN}^+$ and $V_{IN}^-$. The differential input signal is then integrated for a fixed time period, which is 2000 counts (4000 clock periods). The externally-set clock frequency is divided by two before clocking the internal counters. The integration time period is:

$$t_{INT} = \frac{4000}{f_{OSC}}$$

The differential input voltage must be within the device's common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, as in battery-powered applications, $V_{IN}^-$ should be tied to analog common.

Polarity is determined at the end of signal integration phase. The sign bit is a "true polarity" indication in that signals less than 1 LSB are correctly determined. This allows precision null detection that is limited only by device noise and auto-zero residual offsets.

## TC820

### Reference Integrate (Deintegrate) Phase

The reference capacitor, which was charged during the auto-zero phase, is connected to the input of the integrating amplifier. The internal sign logic ensures the polarity of the reference voltage is always connected in the phase opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate determined by the reference potential.

The amount of time required ($T_{DEINT}$) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor ($V_{INT}$) during the integration phase:

$$t_{DEINT} = \frac{R_{INT}\,C_{INT}\,V_{INT}}{V_{REF}}$$

The digital reading displayed by the TC820 is:

$$\text{Digital Count} = 2000\ \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

### System Timing

The oscillator frequency is divided by 2 prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 8000 (4000) counts or 16000 clock pulses. The 8000 count phase is independent of input signal magnitude or polarity.

Each phase of the measurement cycle has the following length:

| Conversion Phase | Counts |
| --- | --- |
| 1) Auto-Zero: | 1500 |
| 2) Signal Integrate:[1,2] | 2000 |
| 3) Reference Integrate: | 1 to 4001 |
| 4) Integrator Output Zero: | 499 to 4499 |

**NOTES:** 1. This time period is fixed. The integration period for the TC820 is:

$$t_{INT\ (TC820)} = \frac{4000}{f_{OSC}} = 2000\ \text{counts}$$

where $f_{OSC}$ is the clock oscillator frequency.

2. Times shown are the RANGE/FREQ at logic low (normal operation). When RANGE/FREQ is logic high, signal integrate times are 200 counts. See "10:1 Range Change" section.

### Input Overrange

When the analog input is greater than full scale, the LCD will display "OL" and the "OVERRANGE" LCD annunciator will be on.

### Peak Reading Hold

The TC820 provides the capability of holding the highest (or peak) reading. Connecting the PK HOLD input to $V_{DD}$ enables the peak hold feature. At the end of each conversion the contents of the TC820 counter is compared to the contents of the display register. If the new reading is higher than the reading being displayed, the higher reading is transferred to the display register. A "higher" reading is defined as the reading with the higher absolute value.

The peak reading is held in the display register so the reading will not "droop" or slowly decay with time. The held reading will be retained until a higher reading occurs, the PK HOLD input is disconnected from $V_{DD}$, or power is removed.

The peak signal to be measured must be present during the TC820 signal integrate period. The TC820 does not perform transient peak detection of the analog input signal. However, in many cases, such as measuring temperature or electric motor starting current, the TC820 "acquisition time" will not be a limitation. If true peak detection is required, a simple circuit will suffice. See the applications section for details.

The peak reading function is also available when the TC820 is in the frequency counter mode. The counter auto-ranging feature is disabled when peak reading hold is selected.

### 10:1 Range Change

The analog input full-scale range can be changed with the RANGE/FREQ input. Normally, RANGE/FREQ is held low by an internal pulldown. Connecting this pin to $V_S^+$ will increase the full-scale voltage by a factor of 10. No external component changes are required.

The RANGE/FREQ input operates by changing the integrate period. When RANGE/FREQ is connected to $V_{DD}$, the signal integration phase of the conversion is reduced by a factor of 10 (i.e., from 2000 counts to 200 counts).

For the TC820, the 10:1 range change will result in ±4V full scale. This full-scale range will exceed the common-mode range of the input buffer when operating from a 9V battery. If range changing is required for the TC820, a higher supply voltage can be provided or the input voltage can be divided by 2 externally.

### Frequency Counter

In addition to serving as an analog-to-digital converter, the TC820 internal counter can also function as a frequency counter (Figure 4). In the counter mode, pulses at the RANGE/FREQ input will be counted and displayed.

The frequency counter derives its time base from the clock oscillator. The counter time base is:

$$t_{COUNT} = \frac{f_{OSC}}{40,000}$$

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Thus, the counter will operate with a 1-second time base when a 40 kHz oscillator is used. The frequency counter accuracy is determined by the oscillator accuracy. For accurate frequency measurements, a crystal oscillator is recommended.

The frequency counter will automatically select the proper range. Auto-range operation extends over four decades, from 3.999 kHz to 3.999 MHz. Decimal points are set automatically in the frequency mode (Figure 5).

The logic switching levels of the RANGE/FREQ input are CMOS levels. For best counter operation, an external buffer is recommended. See the applications section for details.

## Logic Probe

The TC820 can also function as a simple logic probe (Figure 6). This mode is selected when the LOGIC input is high. Two dual-purpose pins, which normally control the decimal points, are used as logic inputs. Connecting either input to a logic high level will turn on the corresponding LCD annunciator. When the "low" annunciator is on the buzzer will be on. As with the frequency counter input, external level shifters/buffers are recommended for the logic probe inputs.

When the logic probe function is selected while FREQ/$\overline{\text{VOLTS}}$ is low (A/D mode), the ADC will remain in the auto-zero mode. The LCD will read "OL" and all decimal points will be off (Figure 7).

If the logic probe is active while FREQ/$\overline{\text{VOLTS}}$ is high (counter mode), the frequency counter will continue to operate. The display will read "OL" but the decimal points will be visible. If the logic probe input is also connected to the RANGE/FREQ input, bringing the LOGIC input low will immediately display the frequency at the logic probe input.

## Analog Pin Functional Description

### Differential Signal Inputs ($V_{IN}^+$), ($V_{IN}^-$)

The TC820 is designed with true differential inputs, and accepts input signals within the input stage common-mode voltage ($V_{CM}$) range. The typical range is $V_{DD}$ –1V to $V_{SS}$ +1.5V. Common-mode voltages are removed from the system when the TC820 operates from a battery or floating power source (isolated from measured system) and $V_{SS}$ is connected to analog common. (See Figure 8.)
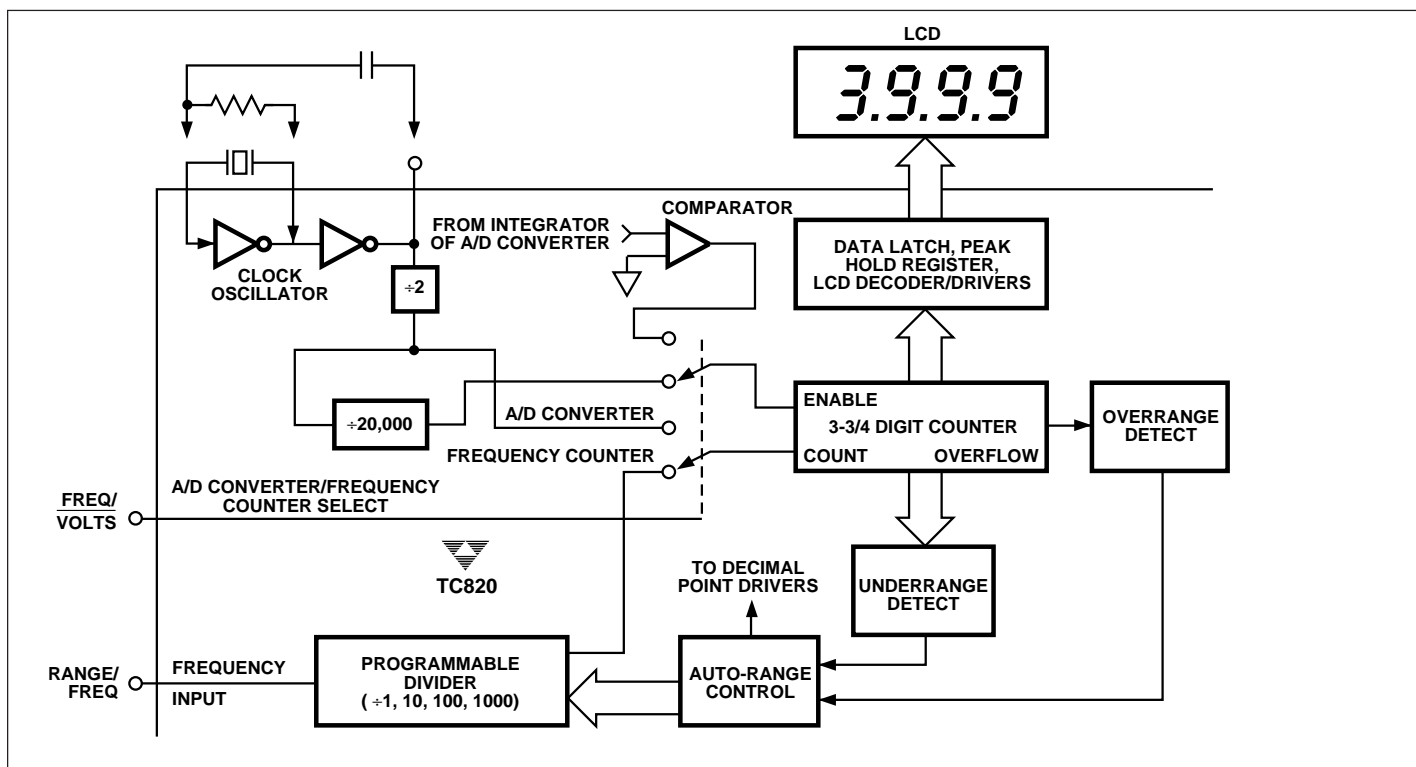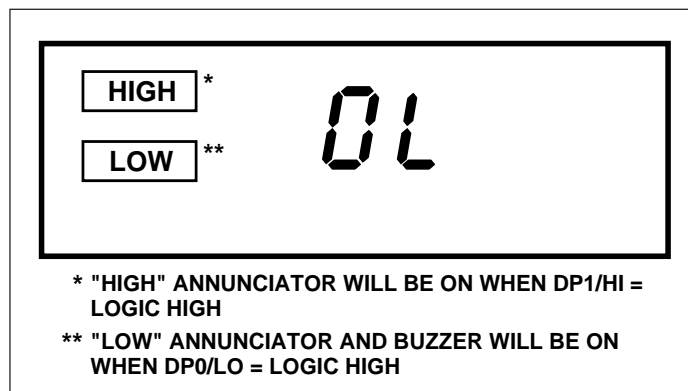
**3**



**Figure 4. TC820 Counter Operation**

**TC820**



| $f_{IN}$ | DECIMAL POINT |
|---|---|
| 0Hz – 3999Hz | DP3 |
| 4kHz – 39.99kHz | DP2 |
| 40kHz – 399.9kHz | DP1 |
| ≥ 400kHz | NONE |

**Figure 5. TC820 Auto-Range Decimal Point Selection vs Frequency Counter Input**

In systems where common-mode voltages exist, the 86dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worst-case condition exists if a large, positive $V_{CM}$ exists in conjunction with a full-scale, negative differential signal. The negative signal drives the integrator output positive along with $V_{CM}$ (Figure 9). For such applications, the integrator output swing can be reduced below the recommended 2V full-scale swing. The integrator output will swing within 0.3V of $V_{DD}$ or $V_{DD}$ without increased linearity error.

### Reference ($V_{DD}$, $V_{SS}$)

The TC820 reference, like the analog signal input, has true differential inputs. In addition, the reference voltage can be generated anywhere within the power supply voltage of the converter. The differential reference inputs permit ratiometric measurements and simplify interfacing with sensors, such as load cells and temperature sensors.



**Figure 6.  Logic Probe Simplified Schematic**

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**Figure 7. LCD During Logic Probe Operation**

* "HIGH" ANNUNCIATOR WILL BE ON WHEN DP1/HI = LOGIC HIGH

** "LOW" ANNUNCIATOR AND BUZZER WILL BE ON WHEN DP0/LO = LOGIC HIGH

To prevent roll-over-type errors from being induced by large common-mode voltages, $C_{REF}$ should be large compared to stray node capacitance. A 0.1µF capacitor is typical.

The TC820 offers a significantly improved analog common temperature coefficient, providing a very stable voltage suitable for use as a voltage reference. The temperature coefficient of analog common is typically 35ppm/°C.

### Analog Common

The analog common pin is set at a voltage potential approximately 3.3V below $V_{DD}$. This potential is guaranteed to be between 3.15V and 3.45V below $V_{DD}$. Analog common is tied internally to an N-channel FET capable of sinking 3mA. This FET will hold the common line at 3.3V below $V_{DD}$ should an external load attempt to pull the common line toward $V_{DD}$. Analog common source current is limited to 12µA, and is therefore easily pulled to a more negative voltage (i.e., below $V_{DD} - 3.3V$).

The TC820 connects the internal $V_{IN}^+$ and $V_{IN}^-$ inputs to analog common during the auto-zero cycle. During the reference integrate phase, $V_{IN}^-$ is connected to analog common. If $V_{IN}^-$ is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converter's 86dB common-mode rejection ratio. In battery-powered applications, analog common and $V_{IN}^-$ are usually connected, removing common-mode voltage concerns. In systems where $V_{IN}^-$ is connected to the power supply ground or to a given voltage, analog common should be connected to $V_{IN}^-$.

The analog common pin serves to set the analog section reference or common point. The TC820 is specifically designed to operate from a battery or in any measurement
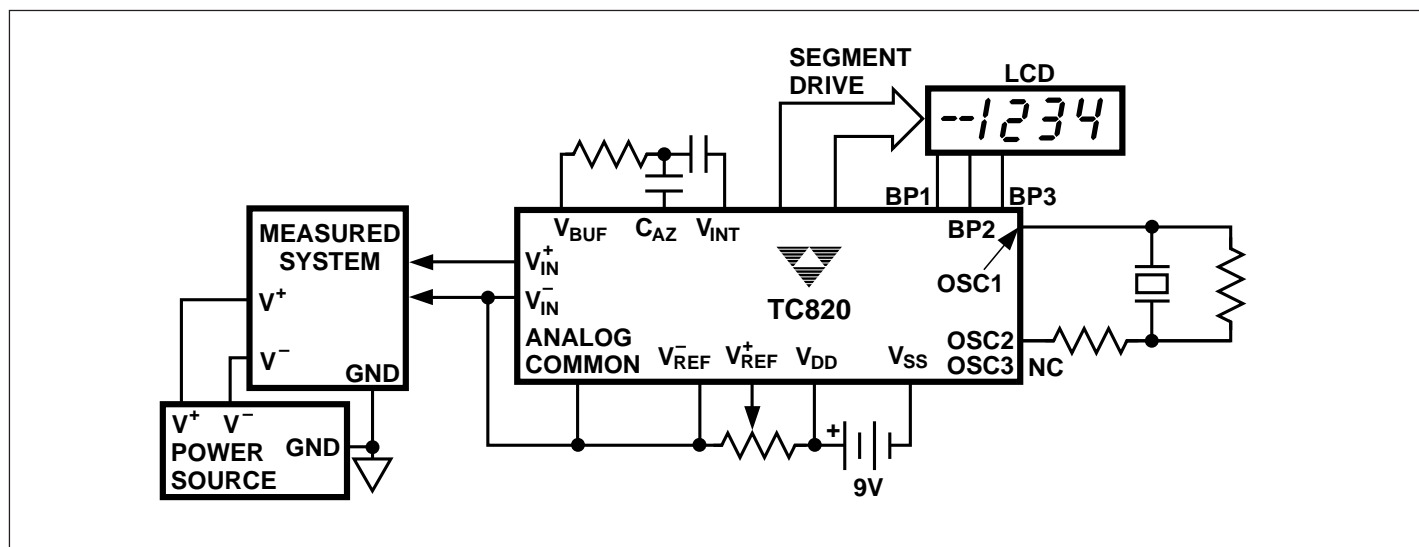


**Figure 8. Common-Mode Voltage Removed in Battery Operation With $V_{IN}^-$ = Analog Common**

**TC820**



$$V_I = \frac{T_I}{R_I C_I} \left[ V_{CM} - V_{IN} \right]$$

**Where:**

$T_I$= Integration Time = $\frac{4000}{f_{OSC}}$

$C_I$= Integration Capacitor

$R_I$= Integration Resistor
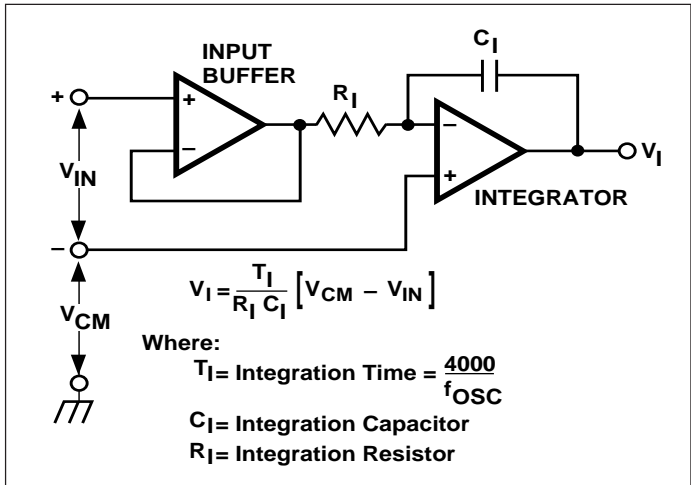
**Figure 9.   Common-Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$)**

system where input signals are not referenced (float) with respect to the TC820 power source. The analog common potential of $V_{DD}$ – 3.3V gives a 7V end-of-battery-life voltage. The analog common potential has a voltage coefficient of 0.001%/%.

With a sufficiently high total supply voltage ($V_{DD}$ – $V_{SS}$ > 7V), analog common is a very stable potential with excellent temperature stability (typically 35ppm/°C). This potential can be used to generate the TC820 reference voltage. An external voltage reference will be unnecessary in most cases, because of the 35ppm/°C temperature coefficient. See the applications section for details.

## Function Control Input Pin Functional Description

The TC820 operating modes are selected with the function control inputs. The control input truth table is shown in Table I. The high logic threshold is ≥ $V_{DD}$ - 1.5V and the low logic level is ≤ DGND +1.5V.

**Table I.  TC820 Control Input Truth Table**

| Logic Input | | | |
|---|---|---|---|
| FREQ/ VOLTS | RANGE/ FREQ | LOGIC | TC820 Function |
| X | X | 1 | Logic Probe |
| 0 | 0 | 0 | A/D Converter, $V_{FULL\ SCALE}$ = 2 × $V_{REF}$ |
| 0 | 1 | 0 | A/D Converter, $V_{FULL\ SCALE}$ = 20 × $V_{REF}$ |
| 1 | Frequency Counter Input | 0 | Frequency Counter |

**NOTES:**  1.  Logic "0" = DGND
2.  Logic "1" = $V_{DD}$

## FREQ/$\overline{VOLTS}$

This input determines whether the TC820 is in the analog-to-digital conversion mode or in the frequency counter mode. When FREQ/$\overline{VOLTS}$ is connected to $V_{DD}$, the TC820 will measure frequency at the RANGE/FREQ input. When unconnected, or connected to DGND, the TC820 will operate as an analog-to-digital converter. This input has an internal 5μA pull-down to DGND.

## LOGIC

The LOGIC input is used to activate the logic probe function. When connected to $V_{DD}$, the TC820 will enter the logic probe mode. The LCD will show "OL" and all decimal points will be off. The decimal point inputs directly control "high" and "low" display annunciators. When LOGIC is unconnected, or connected to DGND, the TC820 will perform analog-to-digital or frequency measurements as selected by the FREQ/$\overline{VOLTS}$ input. The LOGIC input has an internal 5 μA pull-down to DGND.

## RANGE/FREQ

The function of this dual-purpose pin is determined by the FREQ/$\overline{VOLTS}$ input. When FREQ/$\overline{VOLTS}$ is connected to $V_{DD}$, RANGE/FREQ is the input for the frequency counter function. Pulses at this input are counted with a time base equal to $f_{OSC}$/40,000. Since this input has CMOS input levels ($V_{DD}$ - 1.5V and DGND +1.5V), an external buffer is recommended.

When the TC820 analog-to-digital converter function is selected, connecting RANGE/FREQ to $V_{DD}$ will divide the integration time by 10. Therefore, the RANGE/FREQ input can be used to perform a 10:1 range change without changing external components.

## DP0/LO, DP1/HI

The function of these dual-purpose pins is determined by the LOGIC input. When the TC820 is in the analog-to-digital converter mode, these inputs control the LCD decimal points. The decimal point truth table is shown in Table II. These inputs have internal 5μA pull-downs to DGND when the voltage/frequency measurement mode is active.

**Table II.  TC820 Decimal Point Truth Table**

| Decimal Point Inputs | | |
|---|---|---|
| DP1 | DP0 | LCD |
| 0 | 0 | 3999 |
| 0 | 1 | 399.9 |
| 1 | 0 | 39.99 |
| 1 | 1 | 3.999 |

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Connecting the LOGIC input to $V_{DD}$ places the TC820 in the logic probe mode. In this mode, the DP0/LO and DP1/HI inputs control the LCD "low" and "high" annunciators directly. When DP1/HI is connected to $V_{DD}$, the "high" annunciator will turn on. When DP0/LO is connected to $V_{DD}$, the "low" annunciator and the buzzer will turn on. The internal pull-downs on these pins are disabled when the logic probe function is selected.

These inputs have CMOS logic switching thresholds. For optimum performance as a logic probe, external level shifters are recommended. See the applications section for details.

### BUZ IN

This input controls the TC820 on-chip buzzer driver. Connecting BUZ IN to $V_{DD}$ will turn the buzzer on. There is an external pull-down to DGND. BUZ IN can be used with external circuitry to provide additional functions, such as a fast, audible continuity indication.

## Additional Features

The TC820 is available in 40-pin and 44-pin packages. Several additional features are available in the 44-pin package.

### $\overline{EOC}$/HOLD

$\overline{EOC}$/HOLD is a dual-purpose, bidirectional pin. As an output, this pin goes low for 10 clock cycles at the end of each conversion. This pulse latches the conversion data into the display driver section of the TC820.

$\overline{EOC}$/HOLD can be used to hold (or "freeze") the display. Connecting this pin to $V_{DD}$ inhibits the display update process. Conversions will continue, but the display will not change. $\overline{EOC}$/HOLD will hold the display reading for either analog-to-digital or frequency measurements.

The input/output structure of the $\overline{EOC}$/HOLD pin is shown in Figure 10. The output drive current is only a few microAmps, so $\overline{EOC}$/HOLD can easily be overdriven by an open-collector logic gate, as well as a FET, bipolar transistor, or mechanical switch. When used as an output, $\overline{EOC}$/HOLD will have a slow rise and fall time due to the limited output current drive. A CMOS Schmitt trigger buffer is recommended.
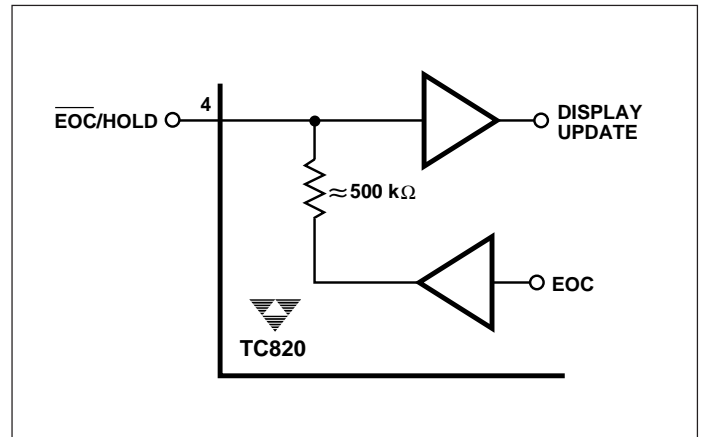


**Figure 10. $\overline{EOC}$/HOLD Pin Schematic**

### Overrange (OR), Underrange (UR)

The OR output will be high when the analog input signal is greater than full scale (3999 counts). The UR output will be high when the display reading is 380 counts or less.

The OR and UR outputs can be used to provide an auto-ranging meter function. By logically ANDing these outputs with the inverted $\overline{EOC}$/HOLD output, a single pulse will be generated each time an underranged or overranged conversion occurs (Figure 11).
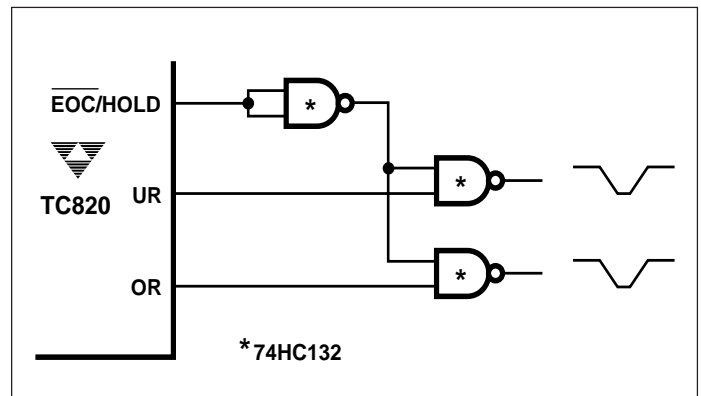


**Figure 11. Generating Underrange and Overrange Pulses**

### $V_{DISP}$

The $V_{DISP}$ input sets the peak-to-peak LCD drive voltage. In the 40-pin package, $V_{DISP}$ is connected internally to DGND, providing a typical LCD drive voltage of $5V_{P-P}$. The 44-pin package includes a separate $V_{DISP}$ input for applications requiring a variable or temperature-compensated LCD drive voltage. See the applications information for suggested circuits.

## TC820

**V<sub>DISP</sub>**

The $V_{DISP}$ input sets the peak-to-peak LCD drive voltage. In the 40-pin package, $V_{DISP}$ is connected internally to DGND, providing a typical LCD drive voltage of 5 $V_{P-P}$. The 44-pin package includes a separate $V_{DISP}$ input for applications requiring a variable or temperature-compensated LCD drive voltage. See the applications information for suggested circuits.

## APPLICATIONS INFORMATION

### Power Supplies

The TC820 is designed to operate from a single power supply such as a 9V battery (Figure 12). The converter will operate over a range of 7V to 15V. For battery operation, analog common (COM) provides a common-mode bias voltage (see analog common discussion in the theory of operation section). However, measurements cannot be referenced to battery ground. To do so will exceed the negative common-mode voltage limit.
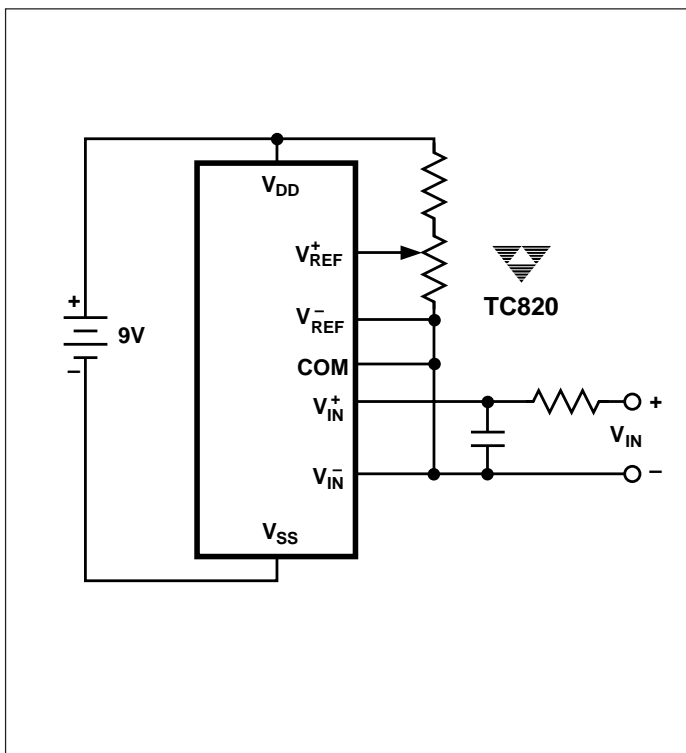


**Figure 12. Powering the TC820 From a Single 9V Battery**

A battery with voltage between 3.5V and 7V can be used to power the TC820, when used with a voltage doubler, as shown in Figure 13. The voltage doubler uses the TC7660 and two external capacitors. With this configuration measurements can be referenced either to Analog Common or to battery ground.

### Digital Ground (DGND)

Digital ground is generated from an internal zener diode (Figure 14). The voltage between $V_{DD}$ and DGND is the internal supply voltage for the digital section of the TC820. DGND will sink a minimum of 3mA.

DGND establishes the low logic level reference for the TC820 mode select inputs, and for the frequency and logic probe inputs. The DGND pin can be used as the negative supply for external logic gates, such as the logic probe buffers. To ensure correct counter operation at high frequency, connect a 1µF capacitor from DGND to $V_{DD}$.

DGND also provides the drive voltage for the LCD. The TC820 40-pin package internally connects the LCD $V_{DISP}$ pin to DGND, and provides an LCD drive voltage of about $5V_{P-P}$. In the 44-pin package, connecting the $V_{DISP}$ pin to DGND will provide a 5V LCD drive voltage.

### Digital Input Logic Levels

Logic levels for the TC820 digital inputs are referenced to $V_{DD}$ and DGND. The high-level threshold is $V_{DD} - 1.5V$ and the low logic level is DGND +1.5V. In most cases, digital inputs will be connected directly to $V_{DD}$ with a mechanical switch. CMOS gates can also be used to control the logic inputs, as shown in the logic probe inputs section.
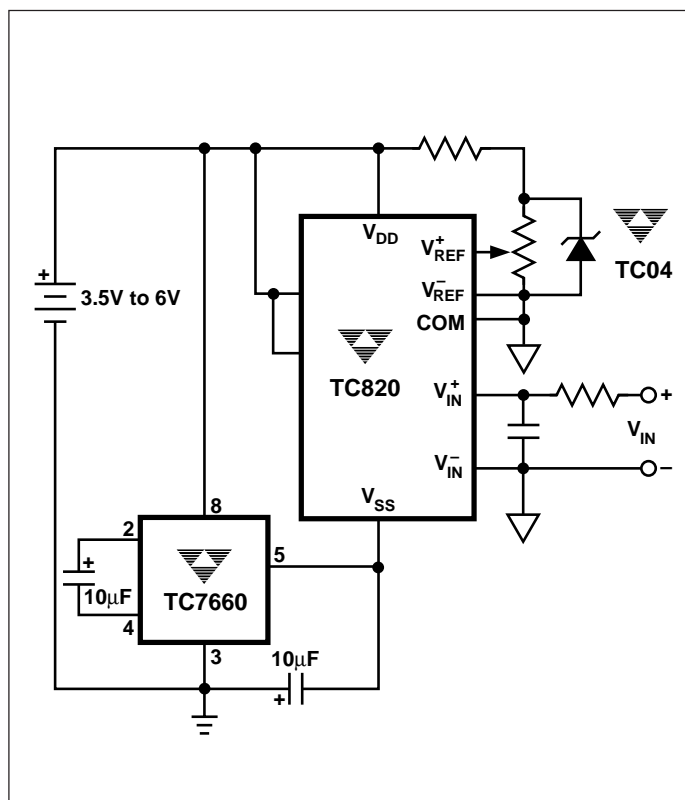


**Figure 13. Powering the TC820 From a Low-Voltage Battery**

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**Figure 14.  DGND and COM Outputs**



**Figure 16.  R-C Oscillator Circuit**
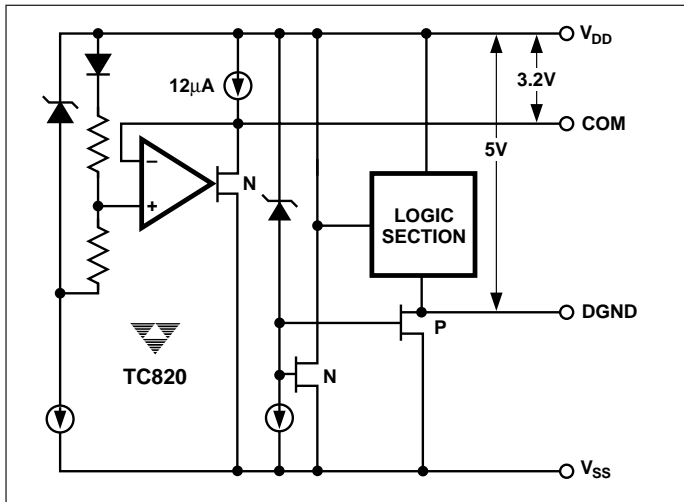
## Clock Oscillator

The TC820 oscillator can be controlled with either a crystal or with an inexpensive resistor-capacitor combination. The crystal circuit, shown in Figure 15, is recommended when high accuracy is required in the frequency counter mode. The 40kHz crystal is a standard frequency for ultrasonic alarms, and will provide a 1-second time base for the counter or 2.5 analog-to-digital conversions per second. Consult the crystal manufacturer for detailed applications information.

Where low cost is important, the R-C circuit of Figure 16 can be used. The frequency of this circuit will be approximately:

$$f_{OSC} = \frac{0.3}{RC}$$



**Figure 15.  Suggested Crystal Oscillator Circuit**

Typical values are $R = 10k\Omega$ and $C = 68pF$. The resistor value should be $\geq 100k\Omega$. For accurate frequency measurement, an R-C oscillator frequency of 40kHz is required.

## System Timing

All system timing is derived from the clock oscillator. The clock oscillator is divided by 2 prior to clocking the A/D counters. The clock is also divided by 8 to drive the buzzer, by 240 to generate the LCD backplane frequency, and by 40,000 for the frequency counter time base. A simplified diagram of the system clock is shown in Figure 17.

## Component Value Selection

### Auto Zero Capacitor — $C_{AZ}$

The value of the auto-zero capacitor ($C_{AZ}$) has some influence on system noise. A 0.47µF capacitor is recommended; a low dielectric absorption capacitor (Mylar) is required.

### Reference Voltage Capacitor — $C_{REF}$

The reference voltage capacitor used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on $C_{REF}$. A 0.1µF capacitor is typical. A good quality, low leakage capacitor (such as Mylar) should be used.

### Integrating Capacitor — $C_{INT}$

$C_{INT}$ should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case, a ±2V integrator output swing is optimum when the analog input is near full scale. For 2.5 readings/second ($f_{OSC} = 40kHz$) and $V_{FS} = 400mV$, a 0.22µF value is suggested. If a different oscillator frequency is used, $C_{INT}$ must be changed in inverse proportion to maintain the
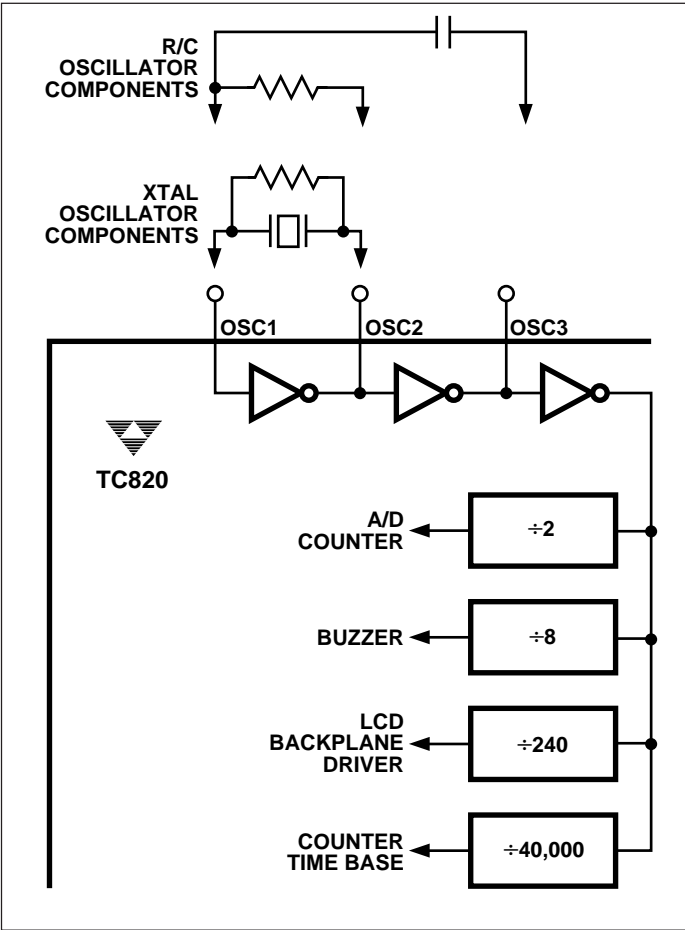
**Figure 17.  System Clock Generation**

nominal ±2V integrator swing. An exact expression for $C_{INT}$ is:

$$C_{INT} = \frac{4000\ V_{FS}}{V_{INT}\ R_{INT}\ f_{OSC}}$$

where:  $f_{OSC}$  = Clock frequency
$V_{FS}$  = Full-scale input voltage
$R_{INT}$  = Integrating resistor
$V_{INT}$  = Desired full-scale integrator output swing

$C_{INT}$ must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

### Integrating Resistor — $R_{INT}$

The input buffer amplifier and integrator are designed with class A output stages. The integrator and buffer can supply 40μA drive currents with negligible linearity errors. $R_{INT}$ is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 400mV full scale, $R_{INT}$ should be about 100kΩ.

## Reference Voltage Selection

A full-scale reading (4000 counts for TC820) requires the input signal be twice the reference voltage.

**Table III.  Reference Voltage Selection**

| Full-Scale Input Voltage ($V_{FS}$) (Note 1) | $V_{REF}$ | Resolution |
|---|---|---|
| 200mV | Note 2 | – |
| 400mV | 200mV | 10 μV |
| 1V | 500mV | 250μV |
| 2V (Notes 3, 4) | 1V | 500μV |

**NOTES:**  1. TC820 in A/D converter mode, RANGE/FREQ = logic low.
2. Not recommended.
3. $V_{FS}$ > 2V may exceed the input common mode range. See "10:1 Range Change" section.
4. Full-scale voltage values are not limited to the values shown. For example, TC820 $V_{FS}$ can be any value from 400mV to 2V.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, that a pressure transducer output is 800mV for 4000 lb/in$^2$. Rather than dividing the input voltage by two, the reference voltage should be set to 400mV. This permits the transducer input to be used directly.

The internal voltage reference potential available at analog common will normally be used to supply the converter's reference voltage. This potential is stable whenever the supply potential is greater than approximately 7V. The low-battery detection circuit and analog common operate from the same internal reference. This ensures that the low-battery annunciator will turn on at the time the internal reference begins to lose regulation.

The TC820 can also operate with an external reference. Figure 18 shows internal and external reference applications.

## Ratiometric Resistance Measurements

The TC820 true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current is passed through the pair (Figure 19). The voltage developed across the unknown is applied to the input and voltages across the known resistor

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## 3-3/4 A/D CONVERTER WITH FREQUENCY COUNTER AND LOGIC PROBE
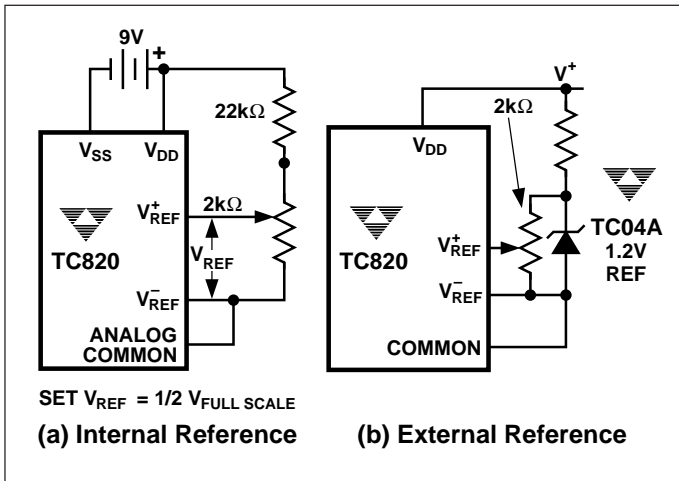


**Figure 18. Reference Voltage Connections**

SET $V_{REF}$ = 1/2 $V_{FULL\ SCALE}$

**(a) Internal Reference**    **(b) External Reference**
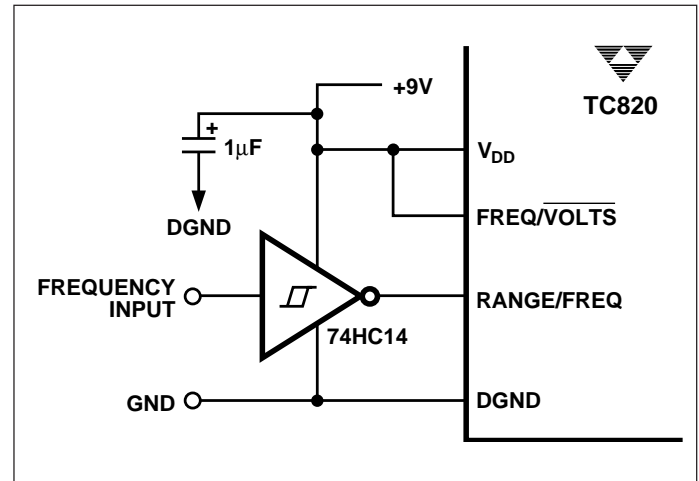
**3**



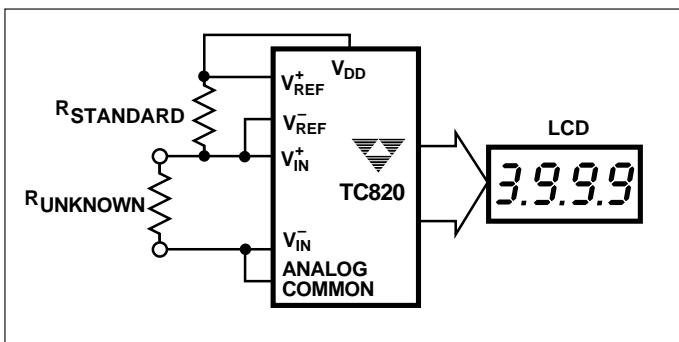**Figure 20. Frequency Counter External Buffer**



**Figure 19. Low Parts Count Ratiometric Resistance Measurement**

applied to the reference input. If the unknown equals the standard, the input voltage will equal the reference voltage and the display will read 2000. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 2000$$

The display will overrange for values of $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

## Buffering the FREQ Input

When the FREQ/$\overline{\text{VOLTS}}$ input is high and the LOGIC input is low, the TC820 will count pulses at the RANGE/FREQ input. The time base will be $f_{OSC}$/40,000, or 1 second with a 40kHz clock. The signal to be measured should swing from $V_{DD}$ to DGND. The RANGE/FREQ input has CMOS input levels without hysteresis. For best results, especially with low-frequency sine-wave inputs, an external buffer with hysteresis should be added. A typical circuit is shown in Figure 20.

## Logic Probe Inputs

The DP0/LO and DP1/HI inputs provide the logic probe inputs when the LOGIC input is high. Driving either DP0/LO or DP1/HI to a logic high will turn on the appropriate LCD annunciator. When DP0/LO is high, the buzzer will be on.

To provide a "single input" logic probe function, external buffers should be used. A simple circuit is shown in Figure 21. This circuit will turn the appropriate annunciator on for high and low level inputs.

If carefully controlled logic thresholds are required, a window comparator can be used. Figure 22 shows a typical circuit. This circuit will turn on the high or low annunciators when the logic thresholds are exceeded, but the resistors connected from DP0/LO and DP1/HI to DGND will turn both annunciators off when the logic probe is unconnected.

The TC820 logic inputs are not latched internally, so pulses of short duration will usually be difficult or impossible to see. To display short pulses properly, the input pulse should be "stretched." The circuit of Figure 22 shows cap-
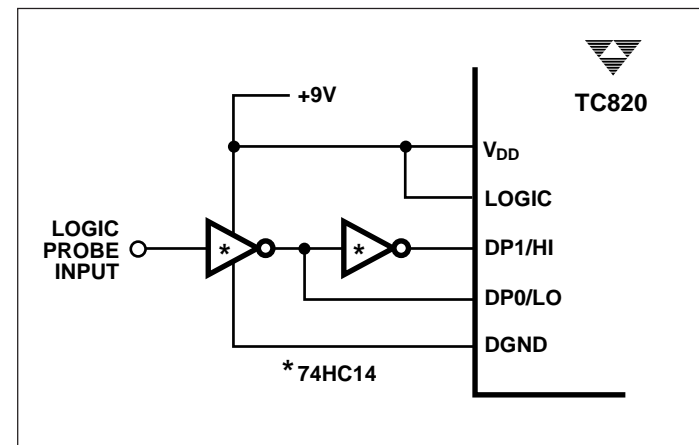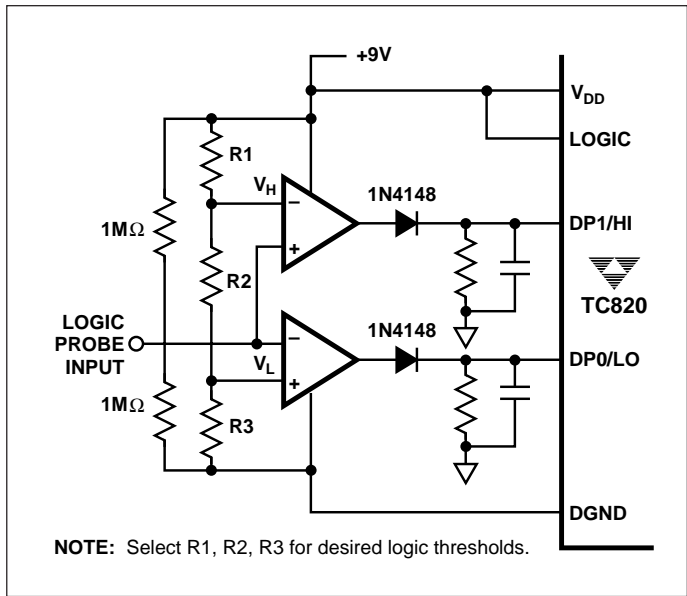


**Figure 21. Simple External Logic Probe Buffer**

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# TC820



**Figure 22. Window Comparator Logic Probe**



**Figure 23. External Peak Detector**

acitors added across the input pull-down resistors to stretch the input pulse and permit viewing short-duration input pulses.

## External Peak Detection

The TC820 will hold the highest A/D conversion or frequency reading indefinitely when the PK HOLD input is connected to $V_{DD}$. However, the analog peak input must be present during the A/D converter's signal integrate period. For slowly changing signals, such as temperature, the peak reading will be properly converted and held.

If rapidly changing analog signals must be held, an external peak detector should be added. An inexpensive circuit can be made from an op amp and a few discrete components, as shown in Figure 23. The droop rate of the external peak detector should be adjusted so that the held voltage will not decay below the desired accuracy level during the converter's 400msec conversion time.

## Liquid Crystal Display (LCD)

The TC820 drives a triplex (multiplexed 3:1) LCD with three backplanes. The LCD can include decimal points, polarity sign, and annunciators for overrange, peak hold, high and low logic levels, and low battery. Table IV shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 240.

Backplane waveforms are shown in Figure 24. These appear on outputs BP1, BP2, and BP3. They remain the same regardless of the segments being driven.

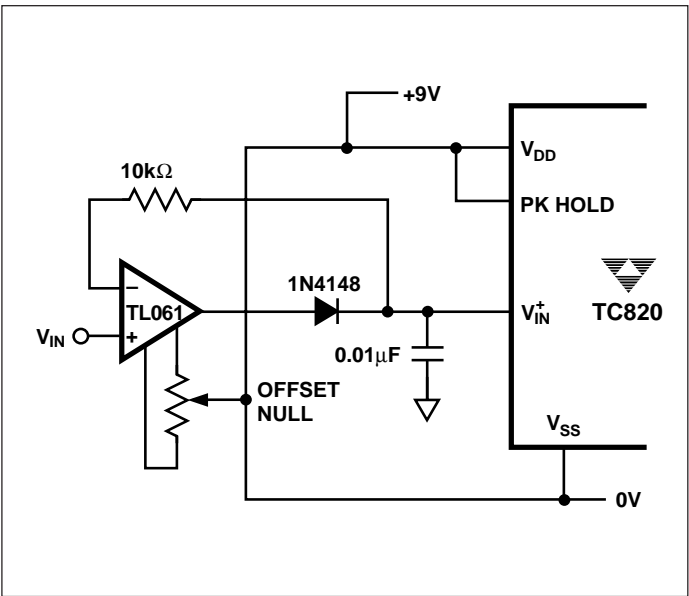Other display output lines have waveforms that vary

depending on the displays values. Figure 25 shows a set of waveforms for the a, g, d outputs of one digit for several combinations of "on" segments.

**Table IV. LCD Backplane and Segment Assignments**

| 40-Pin DIP Pin No. | 44-Pin Flat Pkg Pin No. | LCD Display Pin No. | BP1 | BP2 | BP3 |
|---|---|---|---|---|---|
| 1 | 40 | 3 | LOW | "—" | E4 |
| 2 | 41 | 4 | A4 | G4 | D4 |
| 3 | 42 | 5 | B4 | C4 | DP3 |
| 4 | 43 | 6 | HIGH | F3 | E3 |
| 5 | 44 | 7 | A3 | G3 | D3 |
| 6 | 1 | 8 | B3 | C3 | DP2 |
| 7 | 2 | 9 | OVER | F2 | E2 |
| 8 | 3 | 10 | A2 | G2 | D2 |
| 9 | 4 | 11 | B2 | C2 | DP1 |
| 10 | 5 | 12 | PEAK | F1 | E1 |
| 11 | 6 | 13 | A1 | G1 | D1 |
| 12 | 7 | 14 | B1 | C1 | BATT |
| 13 | 8 | 2,16* | — | — | BP3 |
| 14 | 9 | 1 | — | BP2 | — |
| 15 | 10 | 15 | BP1 | — | — |

*Connect both pins 2 and 16 of LCD to TC820 BP3 output.

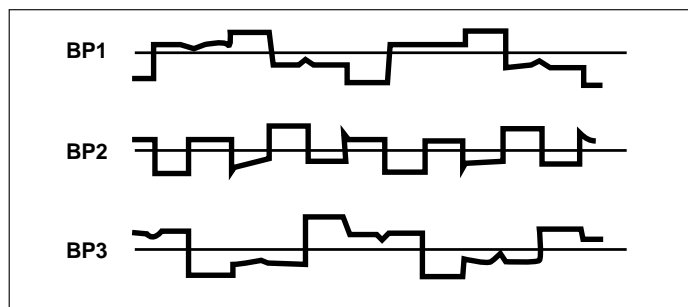▼▼ **TELCOM SEMICONDUCTOR, INC.**

**3**
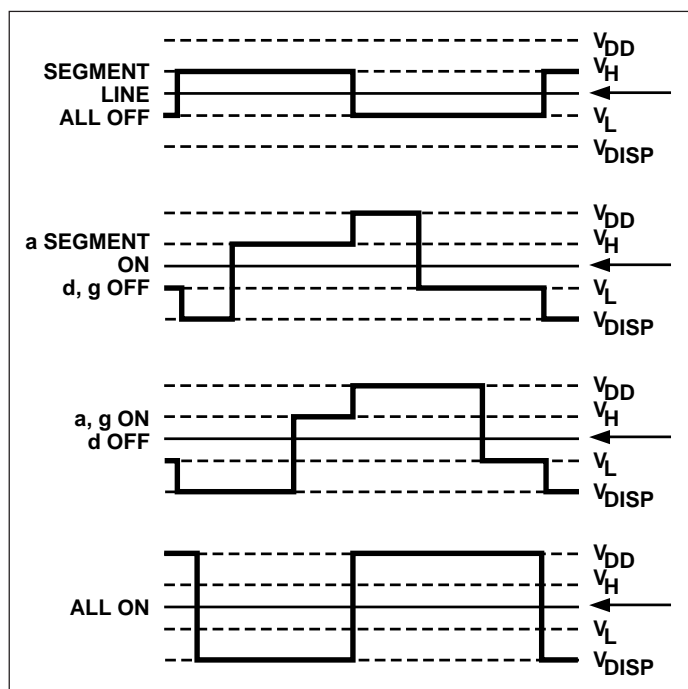


**Figure 24. Backplane Waveforms**



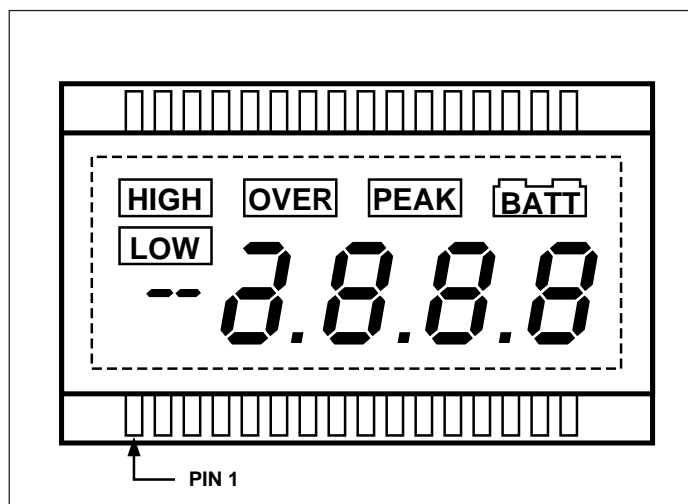**Figure 25. Typical Display Output Waveforms**



**Figure 26. Typical TC820 LCD**

## LCD Source

Although most users will design their own custom LCD, a standard display for the TC820 (Figure 26), Part No. ST-1355-M1, is available from:

Crystaloid (USA)
Crystaloid Electronics
P.O. Box 628
5282 Hudson Dr.
Hudson, OH 44238
Phone: (216) 655-2429
Fax: (216) 655-2176

Crystaloid (Europe)
Rep France
102, rue des Nouvelles
F92150 Suresnes
France
Phone: 33-1-42 04 29 25
Fax: 33-1-45 06 46 99

## Annunciator Output

The annunciator output is a square wave running at the backplane frequency (for example, 167Hz when $f_{OSC} = 40kHz$). The peak-to-peak amplitude is equal to ($V_{DD} - V_{DISP}$). Connecting an annunciator of the LCD to the annunciator output turns it on; connecting it to its backplane turns it off.

## LCD Drive Voltage ($V_{DISP}$)

The peak-to-peak LCD drive voltage is equal to ($V_{DD} - V_{DISP}$). In the 40-pin dual-in-line package (DIP), $V_{DISP}$ is internally connected to DGND, providing a typical LCD drive voltage of $5V_{P-P}$.

For applications with a wide temperature range, some LCDs require that the drive levels vary with temperature to maintain good viewing angle and display contrast. In this case, the TC820 44-pin package provides a pin connection for $V_{DISP}$. Figure 27 shows TC820 circuits that can be adjusted to give a temperature compensation of about 10mV/°C between $V_{DD}$ and $V_{DISP}$. The diode between GND and $V_{DISP}$ should have a low turn-on voltage because $V_{DISP}$ cannot exceed 0.3V below GND.
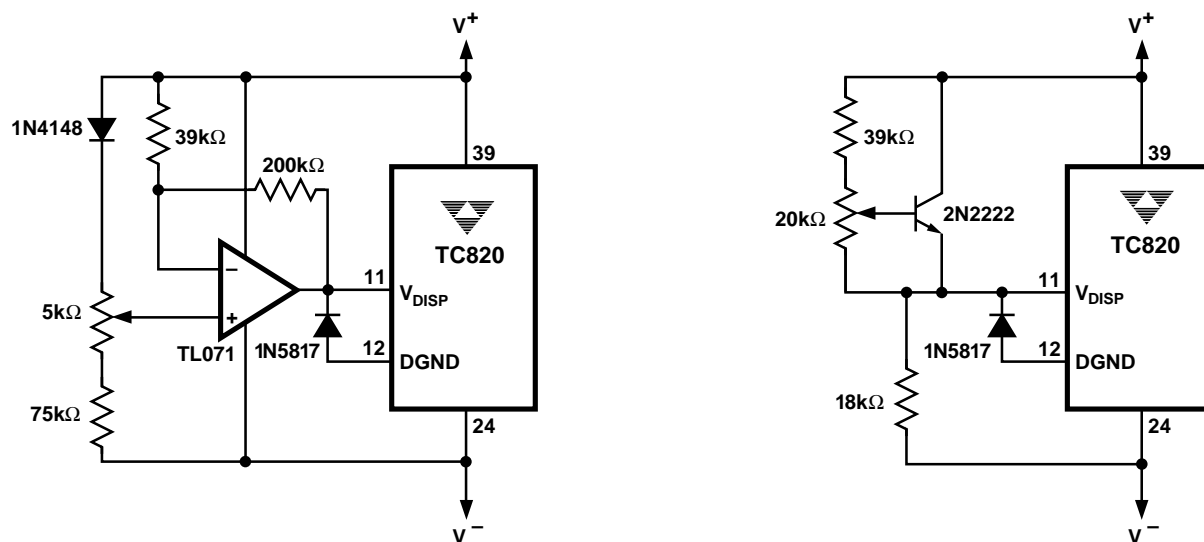
## Crystal Source

Two sources of the 40 kHz crystal are:

Statek Corp.
512 N. Main St.
Orange, CA 92668
Phone: (714) 639-7810
Fax: (714) 997-1256
Part #: CX-1V-40.0

SPK Electronics
2F-1, No. 312, Sec. 4,
   Jen Ai Rd
Taipei, Taiwan R.O.C.
Phone: (02) 754-2677
Fax: 886-2-708-4124
Part#: QRT-38-40.0kHz

▼ **TELCOM SEMICONDUCTOR, INC.**

NOTE: Pin numbers shown are for 44-pin flat package.

**Figure 27. Temperature-Compensating Circuits**